The Impact of Higher Data Rate Requirements on MIPI CSI℠ and MIPI DSI℠ Designs

Brian Daellenbach - Northwest Logic
Ashraf Takla - Mixel
Overview

• The trend towards higher resolution, pixel depth and frame rate cameras and displays is driving the need for higher data rate interfaces.

• The MIPI Alliance Camera Serial Interface (CSI) and Display Serial Interface (DSI) standards are evolving to meet these needs.

• This presentation provides an overview of these trends, the evolving standards, and the corresponding impact on CSI and DSI designs.
Speaker Introduction

• Brian Daellenbach
  • President of Northwest Logic
  • Located in Beaverton, Oregon
  • Controller IP Provider – MIPI, PCIe, DDR/HBM

• Ashraf Takla
  • President of Mixel
  • Located in San Jose, California
  • MIPI PHY Provider – D-PHY, C-PHY, M-PHY

• Together Northwest Logic and Mixel provide a complete, silicon-proven, high-performance, low-power MIPI solution
Camera & Display Trends

**Camera Data Rates**

- 60 Hz, 20 Bit
- 60 Hz, 12 Bit
- 30 Hz, 16 Bit
- 30 Hz, 8 Bit

**Display Data Rates**

- 60 Hz, 36 Bit
- 60 Hz, 30 Bit
- 60 Hz, 24 Bit

Resolution (Megapixels) vs. Total Data Rate (Gbit/s)
MIPI Standards Background

• MIPI Alliance was formed in 2003 to “to benefit the mobile industry by establishing specifications for standard hardware and software interfaces in mobile devices”

• Camera Serial Interface (CSI)
  • Provides a packet-based protocol for interfacing to mobile cameras
  • Widely used

• Display Serial Interface (DSI)
  • Provides a packet-based protocol for interfacing to mobile displays
  • Widely used

• Widespread adoption of these standards in the high-volume mobile market has resulted in low-cost cameras and displays which are being used in other markets also
MIPI PHY Standards

- **D-PHY**
  - N data lanes and 1 clock lane (2 pins per lane)
    - Source synchronous (clock provided separately from the data)
    - Typically 1-4 data lanes are used. 8 infrequently used.
  - Switches between Low Power (LP) and High Speed (HS) modes
    - LP: LVCMOS, HS: Sub-LVDS
  - Widely used in the Camera and Display markets

- **C-PHY**
  - N data lanes (3 pins per lane – also known as trios)
    - Uses 3 phase symbol encoding (2.28 bits/symbol).
    - Clock embedded in each data lane.
    - Typically 1-3 lanes are used to be pin count compatible with D-PHY. More lanes may be used in the future.
  - LP and HS modes
  - Starting to be used in the Camera market

- **M-PHY**
  - SERDES-based standard
  - Not being adopted in the Camera and Display markets yet due to higher cost
# PHY Standard Roadmap

<table>
<thead>
<tr>
<th>Standard</th>
<th>Version</th>
<th>Adopted</th>
<th>Data Rate (Per Lane)</th>
<th>PHY Interface (Per Lane)</th>
</tr>
</thead>
<tbody>
<tr>
<td>D-PHY</td>
<td>1.0</td>
<td>Sep 2009</td>
<td>1.0 Gbit/s</td>
<td>8 bit</td>
</tr>
<tr>
<td></td>
<td>1.1</td>
<td>Dec 2011</td>
<td>1.5 Gbit/s</td>
<td>8 bit</td>
</tr>
<tr>
<td></td>
<td>1.2</td>
<td>Sep 2014</td>
<td>2.5 Gbit/s</td>
<td>8 bit</td>
</tr>
<tr>
<td></td>
<td>2.0</td>
<td>Mar 2016</td>
<td>4.5 Gbit/s</td>
<td>8/16/32 bit</td>
</tr>
<tr>
<td></td>
<td>2.1</td>
<td>~Q4 2016</td>
<td>4.5 Gbit/s</td>
<td>8/16/32 bit</td>
</tr>
</tbody>
</table>

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<tr>
<th>Standard</th>
<th>Version</th>
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<th>Data Rate (Per Trio)</th>
<th>PHY Interface (Per Trio)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C-PHY</td>
<td>1.0</td>
<td>Oct 2014</td>
<td>2.5 Gsym/s</td>
<td>16 bit</td>
</tr>
<tr>
<td></td>
<td>1.1</td>
<td>Feb 2016</td>
<td>2.5 Gsym/s</td>
<td>16/32 bit</td>
</tr>
<tr>
<td></td>
<td>1.2</td>
<td>~Q4 2016</td>
<td>3.5 Gsym/s</td>
<td>16/32 bit</td>
</tr>
</tbody>
</table>

Note: A C-PHY lane is known as a Trio. 1 Sym = 2.28 bits
PHY Standard Data Rates

![Chart showing the total data rates (Gbps) for different years and types of PHYs.]

- D-PHY 4 Lanes
- C-PHY 3 Trios
- C-PHY 4 Trios

YEAR:
- 2009
- 2010
- 2011
- 2012
- 2013
- 2014
- 2015
- 2016
- 2017
## CSI-2 Standard Roadmap

<table>
<thead>
<tr>
<th>Standard</th>
<th>Version</th>
<th>Adopted</th>
<th>PHYs Supported</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSI-2</td>
<td>1.0</td>
<td>Nov 2005</td>
<td>D-PHY 0.58</td>
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<tr>
<td></td>
<td>1.1</td>
<td>Jan 2013</td>
<td>D-PHY 1.1</td>
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<tr>
<td></td>
<td>1.2</td>
<td>Sep 2014</td>
<td>D-PHY 1.2</td>
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<td></td>
<td>1.3</td>
<td>Oct 2014</td>
<td>D-PHY 1.2, C-PHY 1.0</td>
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<tr>
<td></td>
<td>2.0</td>
<td>~Q1 2017</td>
<td>D-PHY 2.1, C-PHY 1.2</td>
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</table>
# DSI/DSI-2 Standard Roadmap

<table>
<thead>
<tr>
<th>Standard</th>
<th>Version</th>
<th>Adopted</th>
<th>PHYs Supported</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSI</td>
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<td>D-PHY 0.65</td>
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<tr>
<td></td>
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<td>D-PHY 1.1</td>
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<td></td>
<td>1.2</td>
<td>Jun 2014</td>
<td>D-PHY 1.1</td>
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<tr>
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<td>1.3</td>
<td>Mar 2015</td>
<td>D-PHY 1.2</td>
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<td>DSI-2</td>
<td>1.0</td>
<td>Jan 2016</td>
<td>D-PHY 2.0, C-PHY 1.1</td>
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<tr>
<td></td>
<td>1.1</td>
<td>TBD</td>
<td>D-PHY 2.1, C-PHY 1.2</td>
</tr>
</tbody>
</table>
Key Design Impacts

• To keep clock rates reasonable, PHYs are evolving from 8 bits/lane to 16 bits/lane
  • Up to D-PHY 1.2 – 8 bits/lane
  • D-PHY 2.0 and beyond – 16 bits/lane
  • C-PHY 1.1 and beyond – 16 bits/lane
  • In the future: 32 bits/lane

• Controllers widths are evolving
  • From: 32 bits width = 4 lanes * 8 bits/lane
  • To: 64 bit width = 4 lanes * 16 bits/lane
  • Results in a wider user interface
  • In the future: 128 bit widths

• PHYs and Controllers are starting to support multi-mode D/C-PHY operation
Clock Rates

The graph illustrates the relationship between clock rates (MHz) and data rates per lane (Gbit/s) for different PPI (Physical Layer Interface) types:

- **D-PHY 8 Bit PPI**
- **D-PHY 16 Bit PPI**
- **D-PHY 32 Bit PPI**
- **C-PHY 16 Bit PPI**
- **C-PHY 32 Bit PPI**

The X-axis represents the data rates per lane in Gbit/s, ranging from 0 to 8. The Y-axis shows the clock rates in MHz, ranging from 0 to 600. The graph indicates a linear increase in clock rates with an increase in data rates per lane.
Mixel PHYs

• Tracking the standards with several generations of silicon-proven D-PHYs
  • 1.0 Gbps -> 1.5 Gbps -> 2.5 Gbps -> D+C-PHY support
• Support range of PHY configurations
  • D-PHY only, D/C-PHY, C-PHY only, M-PHY
• Broad process support
  • 180nm down to 16nm
• Broad foundry support
  • 7 different foundries including TSMC, UMC, GF, SMIC, and others
• Full featured & differentiated solution
  • Low power, small area, high performance, mature, silicon proven
Northwest Logic Controllers

• First Generation
  • CSI-2 and DSI Controller Cores are 32 bits wide

• Second Generation
  • CSI-2 and DSI-2 Controller Cores support both 32 and 64 bit width
  • 32 bit: minimize size and power for lower data rates
  • 64 bit: minimize clock rate for high data rates

• Full featured, high-performance, low power, easy to use

• Delivered as a complete solution integrated and verified with the Mixel PHY
Conclusion

• The trend towards higher resolution, pixel depth and frame rate cameras and displays is driving the need for higher data rate interfaces.
• The MIPI Alliance Camera Serial Interface (CSI) and Display Serial Interface (DSI) standards are evolving to meet these needs.
• These trends will impact MIPI designs in several ways:
  • Higher I/O and clock rates, wider interfaces, use of multi-mode PHYs, use of data compression, etc.
• MIPI designers should consider these trends as they create their product roadmaps and associated designs.
For More Information

• Visit our exhibit in the Grand Hall during the conference.

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