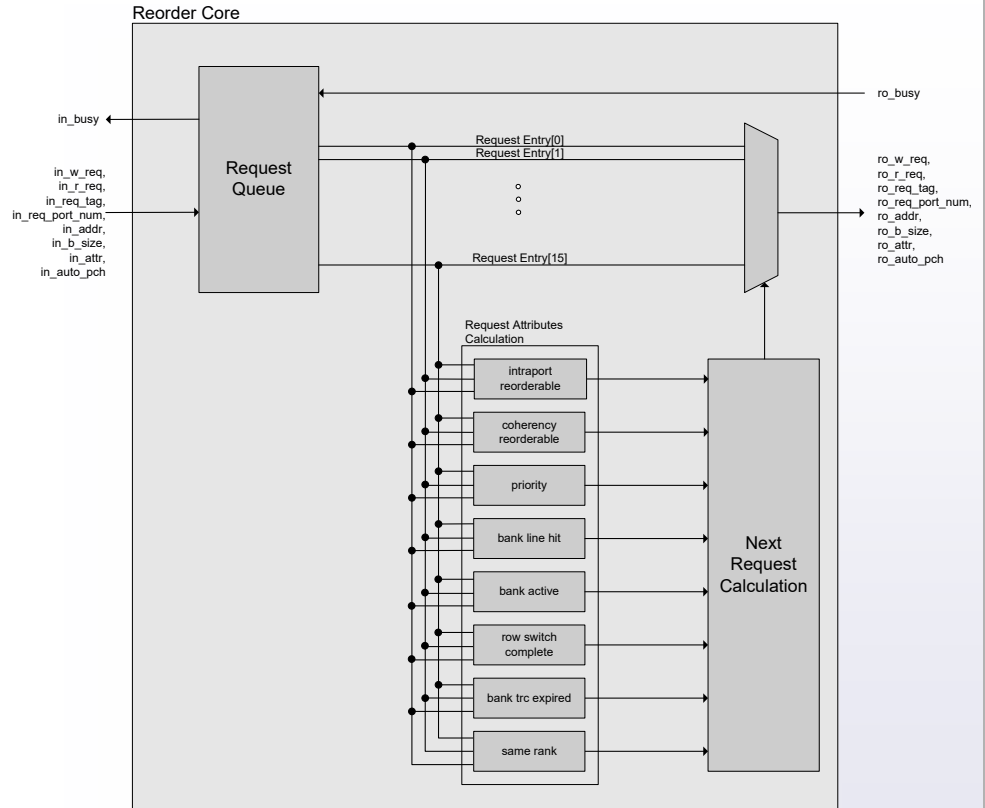


Product Highlights

- Reorders requests based on priority and throughput optimization
- Can be used in single port or multi port configurations
- Option to enforce data coherency during reordering operation
- Option to enable/disable intra-port reordering
- Reorder queue bypassed when empty to minimize latency
- Achieves high clock rates with minimal routing constraints
- Minimal ASIC gate count
- Broad range of ASIC and FPGA platforms supported
- Source code available
- Customization and Integration services available

Block Diagram



Product Overview

The Reorder Core reorders requests based on first on priority and second on throughput optimization.

Throughput optimization includes moving same bank/same row requests next to each other, same bank/ different row requests away from each other, moving reads next to reads and write next to writes.

The core can be used to optionally enforce data coherency by preventing any same row requests from passing over each other.

The core can also optionally disable intra-port (within a port) reordering. Disabling intra-port reordering ensures that the requests on each port are always executed in the same order. In this case only inter-port (between ports) reordering is allowed.

The core can be used in a single port mode or a multi-port mode in conjunction with Northwest Logic's Multi-Port Front-End Core.

To minimize latency, the core's Reorder Queue is bypassed when empty. This enables requests to flow directly through the core when no outstanding requests have been queued up.

Northwest Logic also provides IP Core customization services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Testbench (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates