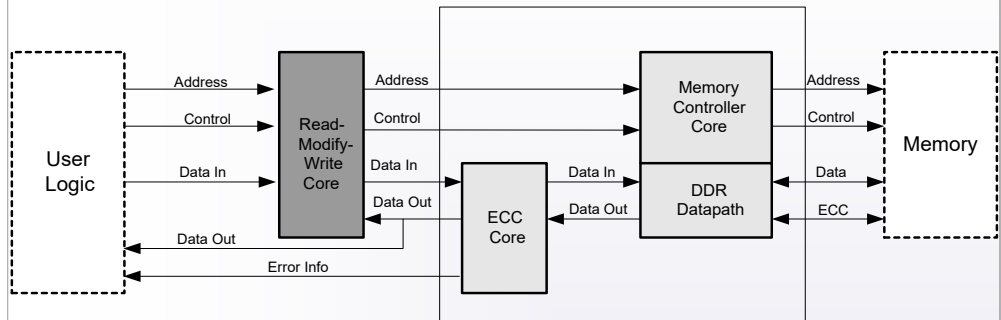


Product Highlights

- Performs Read-Modify-Write (RMW) operations at the start and end of misaligned burst writes when using Error Correction Coding (ECC)
- Performs address translation from byte addressing to the 64-bit or 128-bit addressing of the memory devices
- Automatically breaks long burst requests into multiple requests matching the memory's native burst length
- Prefetch architecture maximizes memory bus efficiency
- Simple user interface signaling (identical to Northwest Logic Memory Controller Cores)
- Minimal ASIC gate count
- Broad range of ASIC and FPGA platforms supported
- Source code available
- Customization and Integration services available

Block Diagram



Product Overview

The Read-Modify-Write (RMW) Core handles misaligned bursts when an Error Correction Code (ECC) is being used.

An ECC code word must be calculated over an entire data word. Misaligned bursts can have partial data words at the front and back end of the burst. To calculate the correct ECC code word, the Read-Modify-Write Core forms the correct starting and ending data words by reading the existing data words and combining them appropriately with the new partial data words.

The core performs address translation from byte addressing to the 64-bit or 128-bit addressing of the memory devices.

The core is provided with the Multi-Burst Core enabling it automatically break long burst requests into multiple requests matching the memory's native burst length

Read-Modify-Write write operations are by their nature inefficient. The Read-Modify-Write Core implements a prefetch architecture that maximizes the memory bus utilization as efficiently as possible.

The core is compatible with memory modules that don't provide Data Mask lines.

Northwest Logic also provides IP Core customization services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Testbench (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates