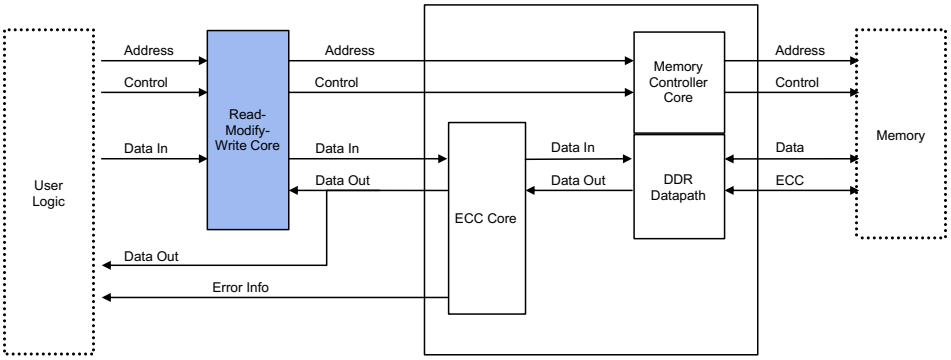
Read-Modify-Write Core

The Northwest Logic Read-Modify-Write (RMW) core handles misaligned bursts when an Error Correction Code (ECC) is being used.

Read-Modify-Write Core Application Example



Overview

Northwest Logic's Read-Modify-Write (RMW) core handles misaligned bursts when an Error Correction Code (ECC) is being used.

An ECC code word must be calculated over an entire data word. Misaligned bursts can have partial data words at the front and back end of the burst. To calculate the correct ECC code word, the Read-Modify-Write core forms the correct starting and ending data words by reading the existing data words and combining them appropriately with the new partial data words.

The core performs address translation from byte addressing to the 64-bit or 128-bit addressing of the memory devices. The core is provided with the Multi-Burst core enabling it to automatically break long burst requests into multiple requests matching the memory's native burst length.

Read-Modify-Write write operations are by their very nature inefficient. The Read-Modify-Write core implements a prefetch architecture that maximizes the memory bus utilization as efficiently as possible.

The core is compatible with memory modules that don't provide Data Mask lines.

Northwest Logic also provides IP core customization services.

Highlights

- Performs RMW operations at the start and end of misaligned burst writes when using ECC
- Performs translation from byte addressing to 64-bit or 128-bit addressing of the memory devices
- Automatically breaks long burst requests into multiple requests matching the memory's native burst length
- Prefetch architecture maximizes memory bus efficiency
- Simple user interface signaling
- Minimal ASIC gate count
- Source code available
- Customization and integration services available

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

rambus.com/controllers