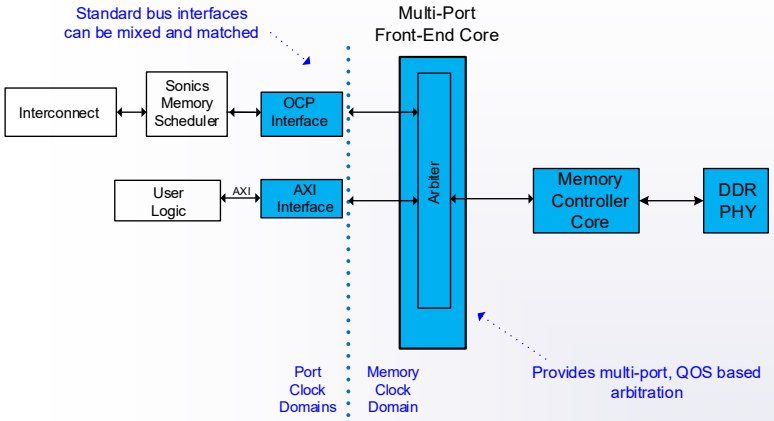
OCP Interface Core

Product Highlights

- Provides high performance interface to OCP
- Handles conversion of bus width/speed to memory width/speed
- Can be used in single port or multi port configurations
- Provided with a Bus Functional Model (testbench)
- Achieves high clock rates with minimal routing constraints
- Minimal ASIC gate count
- Broad range of ASIC and FPGA platforms supported
- Source code available
- Customization and Integration services available

Block Diagram



Product Overview

Northwest Logic's OCP Interface Core is designed for use in applications requiring Open Core Protocol (OCP) interface.

The core accepts write and read requests from a Bus Master. After receiving a write request the core immediately accepts the associated write data enabling the Bus Master to proceed to the next request. The core then arranges for the data to be written into the memory. After receiving a read request, the core arranges for the data to be read from the memory and then provides it to the Bus Master.

The core handles the conversion of the bus width/speed to the memory width/speed. This enables the bus width and speed to be completely independent of the memory width and speed.

The core can be used in a single port configuration connected directly to the Memory Controller Core. Multiple instances of the core can be used with Northwest Logic's Multi-Port Front-End Core. This enables a multi-port design with a mix of different types of bus interfaces to be quickly and easily created.

Northwest Logic also provides the OCP Interface Core with a testbench which serves as a Bus Functional Model.

The OCP Interface Core requires the Read-Modify-Write Core which is licensed separately.

Northwest Logic also provides IP Core customization services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Testbench (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates