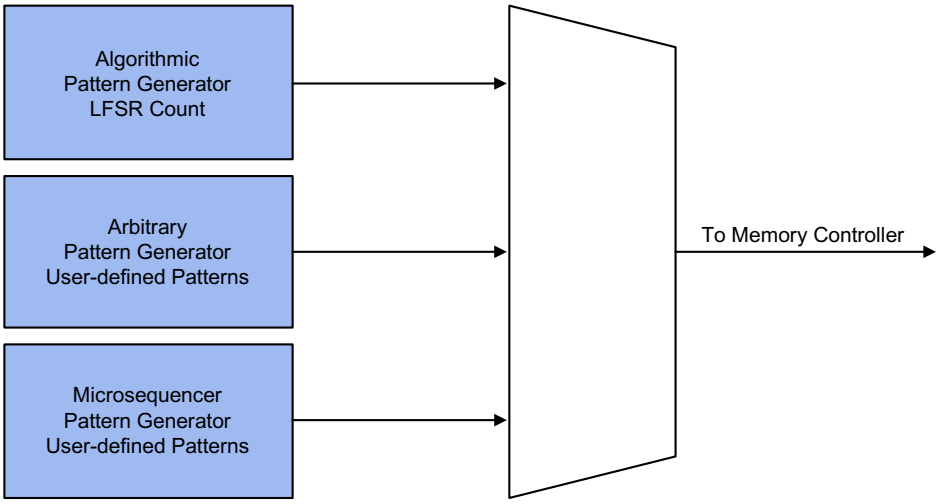
Memory Test Core

The Memory Test core provides comprehensive memory test support for chip and board verification.

Memory Test Core Block Diagram



Overview

Northwest Logic's Memory Test core provides comprehensive memory test support for chip and board validation.

The base version of the core supports walking ones and zeroes, counting, random, and user programmable data patterns. It also supports sequential, random and user programmable address patterns. The random address and data pattern is particularly useful because it can fully stress both the chip and board design.

The Mem Test Analyzer core can be used in conjunction with the Memory Test core to capture the actual and expected test data.

The advanced memory test (AMT) option adds a microsequencer to efficiently generate complex memory test patterns such as MARCH, MATS+, GALPAT, and MOVI. These patterns can be used to isolate memory failures.

AMT is particularly useful for HBM-based memory systems. It includes support for HBM single-bank refresh control, synchronized test execution and parallel memory test RAM loading.

The AMT is provided with example test sequences and an assembler. Users can easily create custom test sequences that can be efficiently executed in the bring-up lab, manufacturing or in field test scenarios.

Highlights

- Part of a comprehensive memory test package with test support for chip and board validation
- Supports walking ones and zeroes, counting and user programmable patterns
- Supports sequential, random and user programmable address patterns
- Advanced memory test support
- Minimal ASIC gate count
- Pipelined design enables timing closure at high clock rates
- Customization and integration services available

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

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