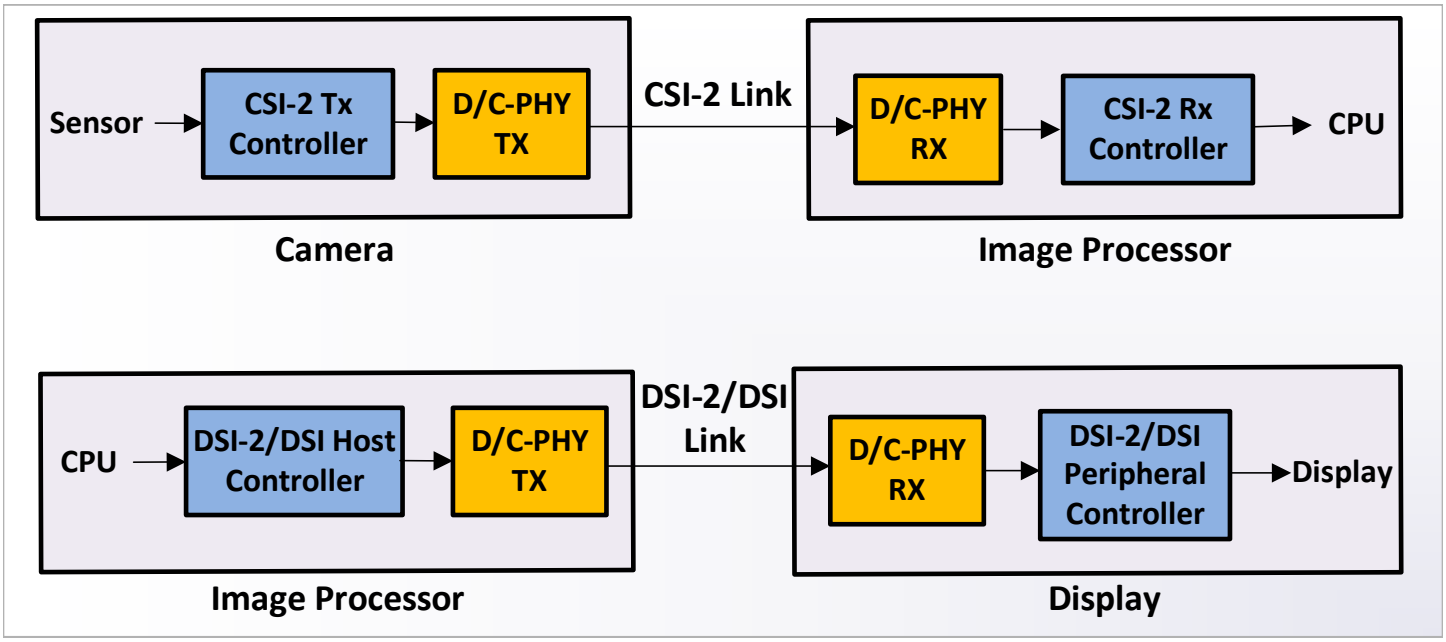
MIPI Solution Overview



Solution Includes:

- **CSI-2 Controller Cores**
  - Fully CSI-2 standard compliant
  - 1-8, 2.5+ Gbit/s D-PHY data lane support
  - 1-4, 2.5+ Gsym/s C-PHY lane (trio) support
  - Support Low Power, High Speed modes
  - Support for all data types
  - Easy to use pixel-based user interface
  - Optional Video Interface

- **DSI-2/DSI Controller Cores**
  - Fully DSI-2/DSI standard compliant
  - 1-4, 2.5+ Gbit/s D-PHY data lane support
  - 1-4, 2.5+ Gsym/s C-PHY lane (trio) support
  - Supports Low Power including Reverse Data and High Speed modes
  - Support for all data types
  - Easy to use packet-based user interface
  - Optional DPI interface

Key Features:

- **Complete Solution**
  - Supports all CSI-2, DSI-2/DSI flavors
  - Transmit (Host) and Receive (Peripheral)
  - Provided with MIPI Testbench
  - Flexible PHY interface supports 8/16/32 bit/lane PPI compatible PHYs
  - Delivered fully integrated and verified with target MIPI PHY
  - Power consumption minimized via clock gating
  - Minimal ASIC gate count
  - Silicon proven

- **High Performance**
  - Supports maximum data rates specified by the CSI-2, DSI-2/DSI standards
  - Minimal latency

- **Easy-To-Use**
  - Simple interface, easy to configure, well-documented

- **Comprehensive Support**
  - ASIC, Structured ASIC and FPGA support
  - Expert technical support provided directly by designers
  - Integration and customization services available

- **MIPI Demo Systems**
  - Complete CSI-2 and DSI FGPA-based demos