The Impact of Higher Data Rate Requirements on MIPI CSI℠ and MIPI DSI℠ Designs

Brian Daellenbach - Northwest Logic
Ashraf Takla - Mixel
Overview

• The trend towards higher resolution, pixel depth and frame rate cameras and displays is driving the need for higher data rate interfaces.
• The MIPI Alliance Camera Serial Interface (CSI) and Display Serial Interface (DSI) standards are evolving to meet these needs.
• This presentation provides an overview of these trends, the evolving standards, and the corresponding impact on CSI and DSI designs.
Speaker Introduction

• Brian Daellenbach
  • President of Northwest Logic
  • Located in Hillsboro, Oregon
  • Controller IP Provider – MIPI, PCIe, DDR/HBM

• Ashraf Takla
  • President of Mixel
  • Located in San Jose, California
  • MIPI PHY Provider – D-PHY, C-PHY, M-PHY

• Together Northwest Logic and Mixel provide a complete, silicon-proven, high-performance, low-power MIPI solution
MIPI Standards Background

- MIPI Alliance was formed in 2003 to “to benefit the mobile industry by establishing specifications for standard hardware and software interfaces in mobile devices”
- Camera Serial Interface (CSI)
  - Provides a packet-based protocol for interfacing to mobile cameras
  - Widely used
- Display Serial Interface (DSI)
  - Provides a packet-based protocol for interfacing to mobile displays
  - Widely used
- Widespread adoption of these standards in the high-volume mobile market has resulted in low-cost cameras and displays which are being used in other markets also
Camera & Display Trends

**Camera Data Rates**

- 60Hz, 20 Bit
- 60Hz, 12 Bit
- 30Hz, 16 Bit
- 30Hz, 8 Bit

**Display Data Rates**

- 60Hz, 36 Bit
- 60Hz, 30 Bit
- 60Hz, 24 Bit

<table>
<thead>
<tr>
<th>Resolution (MegaPixel)</th>
<th>Total Data Rate (Gbit/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HD (1280 x 800)</td>
<td>0.0</td>
</tr>
<tr>
<td>HD (1334 x 750)</td>
<td>0.0</td>
</tr>
<tr>
<td>Full HD (1920 x 1080)</td>
<td>0.0</td>
</tr>
<tr>
<td>Ultra HD (4096 x 2160)</td>
<td>0.0</td>
</tr>
</tbody>
</table>
MIPI PHY Standards

• **D-PHY**
  • N data lanes and 1 clock lane (2 pins per lane)
    • Source synchronous (clock provided separately from the data)
    • Typically 1-4 data lanes are used. 8 infrequently used.
  • Switches between Low Power (LP) and High Speed (HS) modes
    • LP: LVCMOS, HS: Sub-LVDS
  • Widely used in the Camera and Display markets

• **C-PHY**
  • N data lanes (3 pins per lane – also known as trios)
    • Uses 3 phase symbol encoding (2.28 bits/symbol).
    • Clock embedded in each data lane.
    • Typically 1-3 lanes are used to be pin count compatible with D-PHY. More lanes may be used in the future.
  • Low Power (LP) and High Speed (HS) modes
  • Starting to be used in the Camera and Display markets

• **A-PHY**
  • Targeted to automotive market. Transmit up to 15 meters. Standard in development.

• **M-PHY**
  • SERDES-based standard
  • Not being adopted in the Camera and Display markets yet due to higher cost
# PHY Standard Roadmap

<table>
<thead>
<tr>
<th>Standard</th>
<th>Version</th>
<th>Adopted</th>
<th>Data Rate (per lane)</th>
<th>PHY Interface (per lane)</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>D-PHY</td>
<td>1.0</td>
<td>Sep 2009</td>
<td>1.0 Gbit/s</td>
<td>8 bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.1</td>
<td>Dec 2011</td>
<td>1.5 Gbit/s</td>
<td>8 bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.2</td>
<td>Sep 2014</td>
<td>2.5 Gbit/s</td>
<td>8 bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.0</td>
<td>Mar 2016</td>
<td>4.5 Gbit/s</td>
<td>8/16/32 bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.1</td>
<td>Apr 2017</td>
<td>4.5 Gbit/s</td>
<td>8/16/32 bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.0</td>
<td>Q1 2019</td>
<td>TBD</td>
<td>TBD</td>
<td></td>
</tr>
<tr>
<td>C-PHY</td>
<td>1.0</td>
<td>Oct 2014</td>
<td>2.5 Gsym/s</td>
<td>16 bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.1</td>
<td>Feb 2016</td>
<td>2.5 Gsym/s</td>
<td>16/32 bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.2</td>
<td>Apr 2017</td>
<td>3.5 Gsym/s</td>
<td>16/32 bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.0</td>
<td>Q1 2019</td>
<td>TBD</td>
<td>TBD</td>
<td>C-PHY lane is known as a Trio.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Symbol = 2.28 bits.</td>
</tr>
<tr>
<td>A-PHY</td>
<td>1.0</td>
<td>Q1 2020</td>
<td>12 Gbit/s</td>
<td>TBD</td>
<td>Can transmit up to 15 meters</td>
</tr>
</tbody>
</table>
PHY Standard Data Rates

- **D-PHY (4 Lanes)**
- **C-PHY (3 Lanes)**
- **A-PHY (4 Lanes)**
# CSI-2 Standard Roadmap

<table>
<thead>
<tr>
<th>Standard</th>
<th>Version</th>
<th>Adopted</th>
<th>PHYs Supported</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSI-2</td>
<td>1.0</td>
<td>Nov 2005</td>
<td>D-PHY 0.58</td>
</tr>
<tr>
<td></td>
<td>1.1</td>
<td>Jan 2013</td>
<td>D-PHY 1.1</td>
</tr>
<tr>
<td></td>
<td>1.2</td>
<td>Sep 2014</td>
<td>D-PHY 1.2</td>
</tr>
<tr>
<td></td>
<td>1.3</td>
<td>Oct 2014</td>
<td>D-PHY 1.2, C-PHY 1.0</td>
</tr>
<tr>
<td></td>
<td>2.0</td>
<td>Mar 2017</td>
<td>D-PHY 2.1, C-PHY 1.2</td>
</tr>
<tr>
<td></td>
<td>2.1</td>
<td>Apr 2018</td>
<td>D-PHY 2.1, C-PHY 1.2</td>
</tr>
<tr>
<td></td>
<td>3.0</td>
<td>Q1 2019</td>
<td>D-PHY 3.0, C-PHY 2.0</td>
</tr>
</tbody>
</table>
## DSI-2/DSI Standard Roadmap

<table>
<thead>
<tr>
<th>Standard</th>
<th>Version</th>
<th>Adopted</th>
<th>PHYs Supported</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSI</td>
<td>1.0</td>
<td>Apr 2006</td>
<td>D-PHY 0.65</td>
</tr>
<tr>
<td>DSI</td>
<td>1.1</td>
<td>Nov 2011</td>
<td>D-PHY 1.1</td>
</tr>
<tr>
<td>DSI</td>
<td>1.2</td>
<td>Jun 2014</td>
<td>D-PHY 1.1</td>
</tr>
<tr>
<td>DSI</td>
<td>1.3</td>
<td>Mar 2015</td>
<td>D-PHY 1.2</td>
</tr>
<tr>
<td>DSI-2</td>
<td>1.0</td>
<td>Jan 2016</td>
<td>D-PHY 2.0, C-PHY 1.1</td>
</tr>
<tr>
<td>DSI-2</td>
<td>1.1</td>
<td>May 2018</td>
<td>D-PHY 2.0, C-PHY 1.1</td>
</tr>
<tr>
<td>DSI-2</td>
<td>1.2</td>
<td>TBD</td>
<td>D-PHY 2.1, C-PHY 1.2</td>
</tr>
<tr>
<td>DSI-2</td>
<td>TBD</td>
<td>TBD</td>
<td>D-PHY 3.0, C-PHY 2.0</td>
</tr>
</tbody>
</table>
Key Design Impacts

- To keep clock rates reasonable, PHYs are evolving from 8 to 16 to 32 bits/lane
  - PHY data lane rate / PHY data lane width = Controller clock rate
  - Example: 2.5 Gbit/s/lane / 8 bits/lane = 313 MHz clock rate

- This causes the Controllers widths to evolve from 32 to 64 to 128 bit core widths
  - # of lanes * per lane width = Controller core width
  - Example: 4 lanes * 8 bits/lane = 32 bit Controller width

- PHYs and Controllers are starting to support multi-mode D/C-PHY operation
## Controller Clock Rates

<table>
<thead>
<tr>
<th>Standard</th>
<th>Data Rate Per Lane</th>
<th>Clock Rate (8 bit PPI)</th>
<th>Clock Rate (16 bit PPI)</th>
<th>Clock Rate (32 bit PPI)</th>
</tr>
</thead>
<tbody>
<tr>
<td>D-PHY</td>
<td>1.0 Gbit/s</td>
<td>125 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.5 Gbit/s</td>
<td>188 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.5 Gbit/s</td>
<td>313 MHz</td>
<td>156 MHz</td>
<td>78 MHz</td>
</tr>
<tr>
<td></td>
<td>4.5 Gbit/s</td>
<td>563 MHz</td>
<td>281 MHz</td>
<td>141 MHz</td>
</tr>
<tr>
<td>C-PHY</td>
<td>2.5 Gsym/s</td>
<td></td>
<td>356 MHz</td>
<td>178 MHz</td>
</tr>
<tr>
<td></td>
<td>3.5 Gsym/s</td>
<td></td>
<td>499 MHz</td>
<td>249 MHz</td>
</tr>
<tr>
<td>A-PHY</td>
<td>12 Gbit/s</td>
<td></td>
<td>750 MHz</td>
<td>375 MHz</td>
</tr>
</tbody>
</table>
Controller Clock Rates

- D-PHY (8 Bit)
- D-PHY (16 Bit)
- D-PHY (32 Bit)
- C-PHY (16 Bit)
- C-PHY (32 Bit)
- A-PHY (16 Bit)
- A-PHY (32 Bit)
Clock Rate Comments

- Most D-PHY 2.0 and C-PHY 1.1 capable PHYs will support 16 bit PPI
  - We expect 8 bit PPI will be phased out
  - We expect some 32 bit PPI to be used
- D-PHY 2.0 and C-PHY 1.1 are more likely to be used in smaller geometry processes
  - Maximum clock rate is likely to be less an issue
    - There may be exceptions to this where a larger geometry, slower LP process is being targeted
- Over next couple of years, D-PHY and C-PHY data rates will continue to push up
Mixel PHYs

- Tracking the standards with several generations of silicon-proven D-PHYs
  - 1.0 Gbps -> 1.5 Gbps -> 2.5 Gbps -> D+C-PHY support
- Support range of PHY configurations
  - D-PHY only, D/C-PHY, C-PHY only, M-PHY
- Broad process support
  - 180nm down to 16nm
- Broad foundry support
  - 7 different foundries including TSMC, UMC, GF, SMIC, and others
- Full featured & differentiated solution
  - Low power, small area, high performance, mature, silicon proven
Northwest Logic Controllers

• First Generation
  • CSI-2 and DSI Controller Cores are 32 bits wide

• Second Generation
  • CSI-2 and DSI-2 Controller Cores support both 32 and 64 bit width
  • 32 bit: minimize size and power for lower data rates
  • 64 bit: minimize clock rate for high data rates

• Full featured, high-performance, low power, easy to use

• Delivered as a complete solution integrated and verified with the Mixel PHY
Conclusion

• The trend towards higher resolution, pixel depth and frame rate cameras and displays is driving the need for higher data rate interfaces.

• The MIPI Alliance Camera Serial Interface (CSI) and Display Serial Interface (DSI) standards are evolving to meet these needs.

• These trends will impact MIPI designs in several ways:
  • Higher I/O and clock rates, wider interfaces, use of multi-mode PHYs, use of data compression, etc.
  • MIPI designers should consider these trends as they create their product roadmaps and associated designs.
For More Information

• Visit our exhibit in the Grand Hall during the conference.

• Contact Northwest Logic at:
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  • www.mixel.com