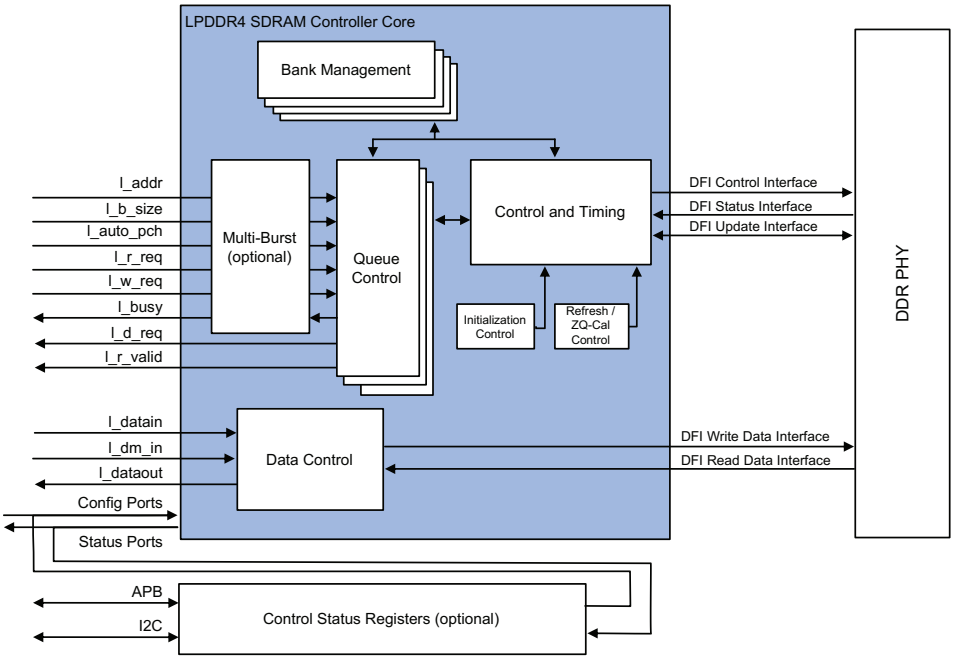
LPDDR4 Controller Core

The Northwest Logic LPDDR4 controller core is designed for use in applications requiring high memory throughput at low power including mobile, Internet of Things (IoT), automotive, laptop PCs, and edge networking devices.

LPDDR4 Controller Core Block Diagram



Highlights

- Maximizes bus efficiency via lookahead command processing, bank management, and auto-precharge
- Minimizes latency via parameterized pipeling
- Supports full-rate, half-rate and quarter-rate clock operation
- Supports LPDDR4 data bus inversion (DBI) and data mask (DM)
- Supports self-refresh, partial array self-refresh, power down, and deep power down modes

Protocol Compatibility

Standards	Data Rates (Gbps)
LPDDR4	3.2 Gbps/pin

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

Northwest Logic's Low Power LPDDR4 Controller Core is designed for use in applications requiring high memory throughput, high clock rates and full programmability.

The core accepts commands using a simple local interface and translates them to the command sequences required by LPDDR4 devices. The core also performs all initialization, refresh and power-down functions.

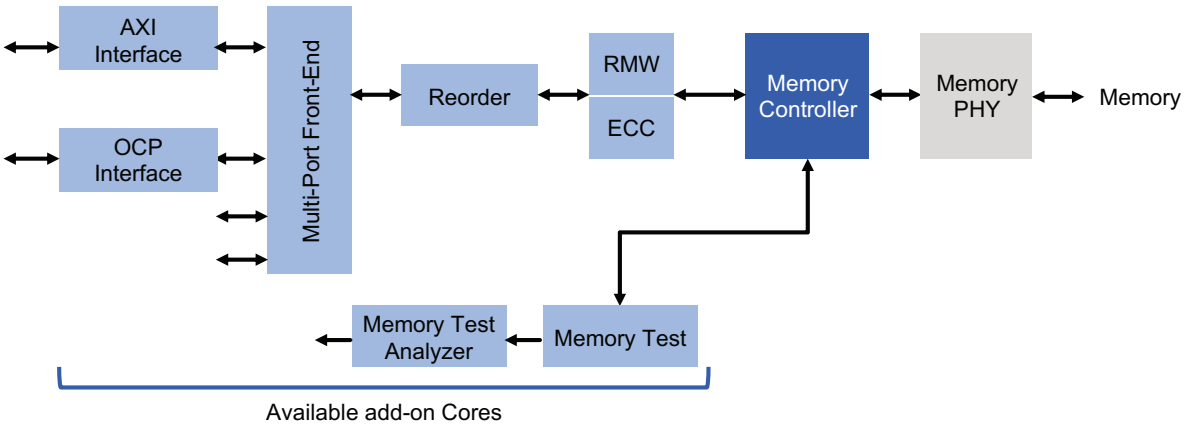
The core uses bank management modules to monitor the status of each LPDDR bank. Banks are only opened or closed when necessary, minimizing access delays.

The core queues up multiple commands in the command queue. This enables optimal bandwidth utilization for both short transfers to highly random address locations as well as longer transfers to contiguous address space. The command queue is also used to opportunistically perform look-ahead activates, precharges and auto-precharges further improving overall throughput.

The core is provided with run-time programmable inputs for all memory timing parameters and configuration settings. This ensures compatibility with all LPDDR4 configurations.

Add-On Cores such as a Multi-Port Front-End and Reorder Core can be optionally delivered with the core. The core is delivered fully integrated and verified with the target DDR PHY.

Add-On Cores



Optional Cores and Services

Add-On cores such as a Multi-Port Front-End, Reorder core or out-of-band ECC core are available as options. Customization and integration services are also available.

Features

- Maximizes bus efficiency via look-ahead command processing, bank management, and auto-precharge
- Latency minimized via parameterized pipelining
- Achieves high clock rates with minimal routing constraints
- Supports full-rate, half-rate and quarter-rate clock operation
- Multi-mode controller support
- Full run-time configurable timing parameters and memory settings
- Supports LPDDR4 data bus inversion (DBI) and data mask (DM)
- Supports self-refresh, partial array self-refresh, power down, and deep power down modes
- DFI compatible
- Full set of Add-On cores available
- Delivered fully integrated and verified with target LPDDR PHY
- Minimal ASIC gate count
- Broad range of ASIC platforms supported
- Source code available
- Customization and integration services available

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