### Product Highlights

- Implements standard DRAM Single Error Correction (SEC) and Double Error Detection (DED) algorithm
- Store Data and ECC in the same memory
- Generates one 8 bit ECC value for each 64 bits of data
- ECC check bytes are distributed throughout memory in “groups” to allow the ECC accesses to normally occur to the same row, bank pair (page) as the user data access that it protects
- Optimally only 1 ECC access is needed to support up to 8 data reads or 8 data writes (88.88% of the GDDR6 bandwidth)
- Error flags indicate what type of error occurred (1-bit or 2-bit)
- Bit position of the error is provided for single-bit errors
- Minimal ASIC gate count
- Source code available

### Block Diagram

![Block Diagram of In-Line ECC Core](image)

### Product Overview

Northwest Logic’s In-Line Error Correction Coding (In-Line ECC) Core is available to be used with Northwest Logic’s GDDR6 Controller Core. The In-Line ECC Core implements the standard Hamming Code based DRAM Single Error Correction (SEC) and Double Error Detection (DED) algorithm. This algorithm generates an 8 bit ECC value for each 64 bits of data.

Since GDDR6 does not support “out-of-band” ECC data protection efficiently, the In-Line ECC Core provides the option to use ~11.2% of the GDDR6 data memory to hold error correcting code bytes that protect the remaining ~88.8 of the GDDR6 data memory. Since this is “In-Line” ECC protection (versus the more typically used out-of-band ECC protection), it also consumes some of the GDDR6 memory data bandwidth to support accessing “In-Line” ECC check bytes and thus delivers slightly less data bandwidth to the user than if ECC protection is not used.

The core consists of an ECC generation path as well as ECC detection and correction. ECC correction is possible for single bit errors occurring in one of combined 72 data and check bits. ECC detection is possible for errors in two of the combined 72 data and check bits.

Various status information is provided to the user including whether an error was detected on a single bit or two bits. The bit position of the error is provided for the case of a single bit errors.

To optimize performance, when using the Reorder Core or Multi-Port Front-End Core, the In-Line ECC core is placed between the Reorder core/Multi-Port Front-End and the GDDR6 controller therefore minimizing the amount of ECC data caching that is needed. When not using the Reorder Core/Multi-Port Front-End, the Inline module is placed between the user interface and the NWL low level GDDR6 controller.

### Product Deliverables:

- Core (Source Code)
- Testbench (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates