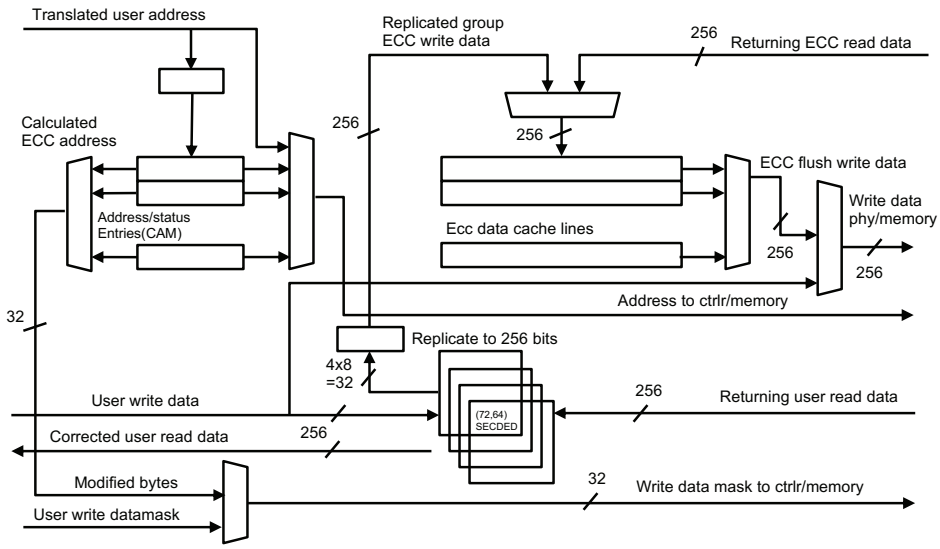
In-Line ECC Core

The Northwest Logic In-Line Error Correction Coding (ECC) core implements standard DRAM Single Error Correction (SEC) and Double Error Detection (DED) algorithm.

In-Line ECC Core Block Diagram



Highlights

- Supports Northwest Logic GDDR6 and LPDDR4 Controller cores
- Implements standard DRAM Single Error Correction (SEC) and Double Error Detection (DED) algorithm
- Generates an 8-bit ECC word for each 64 bits of data
- Error flags indicate what type of error occurred (1-bit or 2-bit)
- Bit position of the error is provided for single-bit errors
- Optimally only 1 ECC access is needed to support up to 8 data reads or 8 data writes (88.9% of data bandwidth)

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic In-Line Error Correction Coding (In-Line ECC) core works with the Northwest Logic GDDR6 and LPDDR4 Controller cores. The In-Line ECC implements the standard Hamming Code-based DRAM Single Error Correction (SEC) and Double Error Detection (DED) algorithm. This algorithm generates an 8-bit ECC value for each 64 bits of data.

Since GDDR6 memory does not support “out-of-band” ECC data protection efficiently, the In-Line ECC core provides the option to use 11.1% of the GDDR6 data memory to hold ECC bytes that protect the remaining 88.9% of data. In-line ECC thus consumes some of the available bandwidth to provide data protection. The same applies for an LPDDR4 implementation.

The core consists of an ECC generation path as well as ECC detection and correction. ECC correction is possible for single-bit errors occurring in one of the combined 72 data and check bits. ECC detection is possible for errors in two of the combined 72 data and check bits.

Various status information is provided to the user including whether an error was detected on a single bit or two bits. The bit position of the error is provided for the case of a single bit error. ECC check bytes are distributed throughout memory in “groups” to allow accesses to normally occur to the same row, bank pair (page) as the user data access that it protects.

To optimize performance, when using the Reorder core or Multi-Port Front-End core, the In-Line ECC core is placed between the GDDR6 (or LPDDR4) controller and the aforementioned cores. This minimizes the amount of ECC data caching that is needed. When not using the Reorder or Multi-Port Front End cores, the In-line ECC core is placed between the user interface and the GDDR6 (or LPDDR4) controller.

Rambus also provides IP core customization services.

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