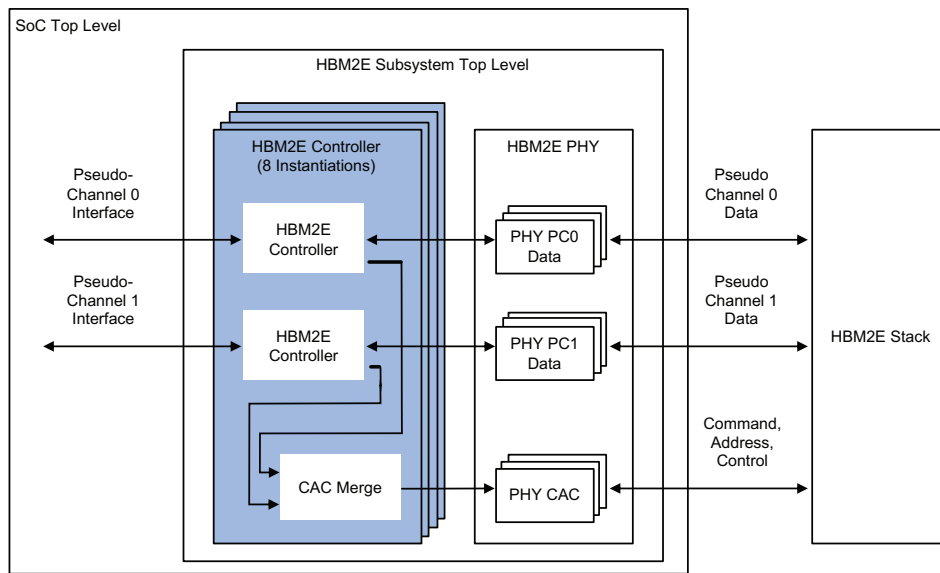


HBM2/2E Controller Core

The Northwest Logic HBM2/2E controller core is designed for use in applications requiring high memory bandwidth and low latency including AI/ML, HPC, data center and graphics.

HBM2E Dual-Controller Configuration



Highlights

- Supports HBM2E and HBM2 devices
- Supports all standard HBM2E channel densities (4, 6, 8, 12, 16, 24 Gb)
- Supports up to 3.2 Gbps/pin
- Maximizes memory bandwidth and minimizes latency via Look-Ahead command processing
- Achieves high clock rates with minimal routing constraints
- DFI compatible (with extensions added for HBM2E)
- Supports AXI, OCP or native interface to user logic

Protocol Compatibility

Standards	Data Rates (Gbps)
HBM2E	0.5 to 3.2
HBM2	0.5 to 2.0

Overview

Northwest Logic’s High Bandwidth Memory generation 2 Evolutionary (HBM2E) Controller Core is designed for use in applications requiring high memory throughput, low latency and full programmability.

The core accepts commands using a simple local interface and translates them to the command sequences required by HBM2/2E devices. The core also performs all initialization, refresh and power-down functions.

The core queues up multiple commands in the command queue. This enables optimal bandwidth utilization for both short transfers to highly random address locations as well as longer transfers to contiguous address space. The command queue is also used to opportunistically perform look-ahead activates, precharges and auto-precharges, further improving overall throughput.

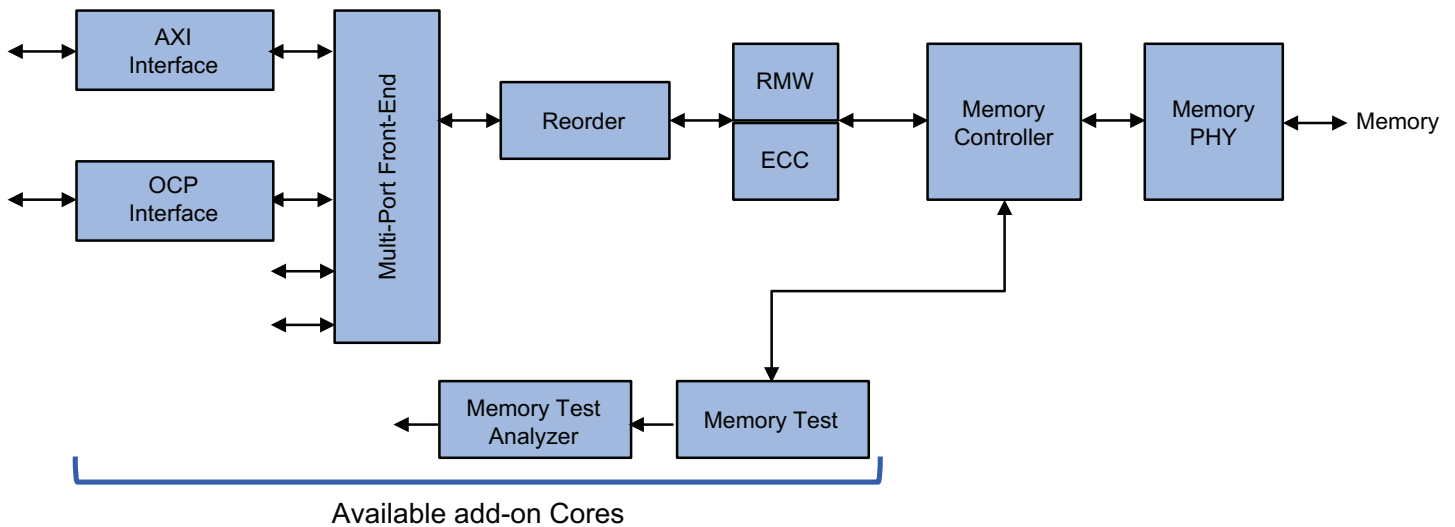
The core supports all HBM2/2E features, including: data bus inversion (DBI), DQ parity, command / address parity modes, and single-bank refresh. Add-On Cores such as a Multi-Port Front-End and Reorder Core can be optionally delivered with the core.

The core is delivered fully integrated and verified with the target HBM2/2E PHY. It has been co-verified with the Rambus HBM2E memory PHY.

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Add-On Cores



Optional Cores and Services

Add-On cores such as a Multi-Port Front-End, Reorder core and out-of-band ECC cores are available as options. Customization and integration services are also available.

Features

- Supports HBM2E and HBM2 devices
- Supports all standard HBM2E channel densities (4, 6, 8, 12, 16, 24 Gb)
- Supports data rates of up to 3.2 Gbps/pin
- Can handle two pseudo-channels with one controller or independently with two controllers
- Queue-based interface optimizes performance and throughput
- Maximizes memory bandwidth and minimizes latency via Look-Ahead command processing
- Achieves high clock rates with minimal routing constraints
- Full run-time configurable timing parameters and memory settings
- DFI compatible (with extensions added for HBM2/2E)
- Full set of Add-on cores available
- Supports AXI, OCP or native interface to user logic
- Delivered fully integrated and verified with target PHY
- Customization and integration services available

rambus.com/controllers