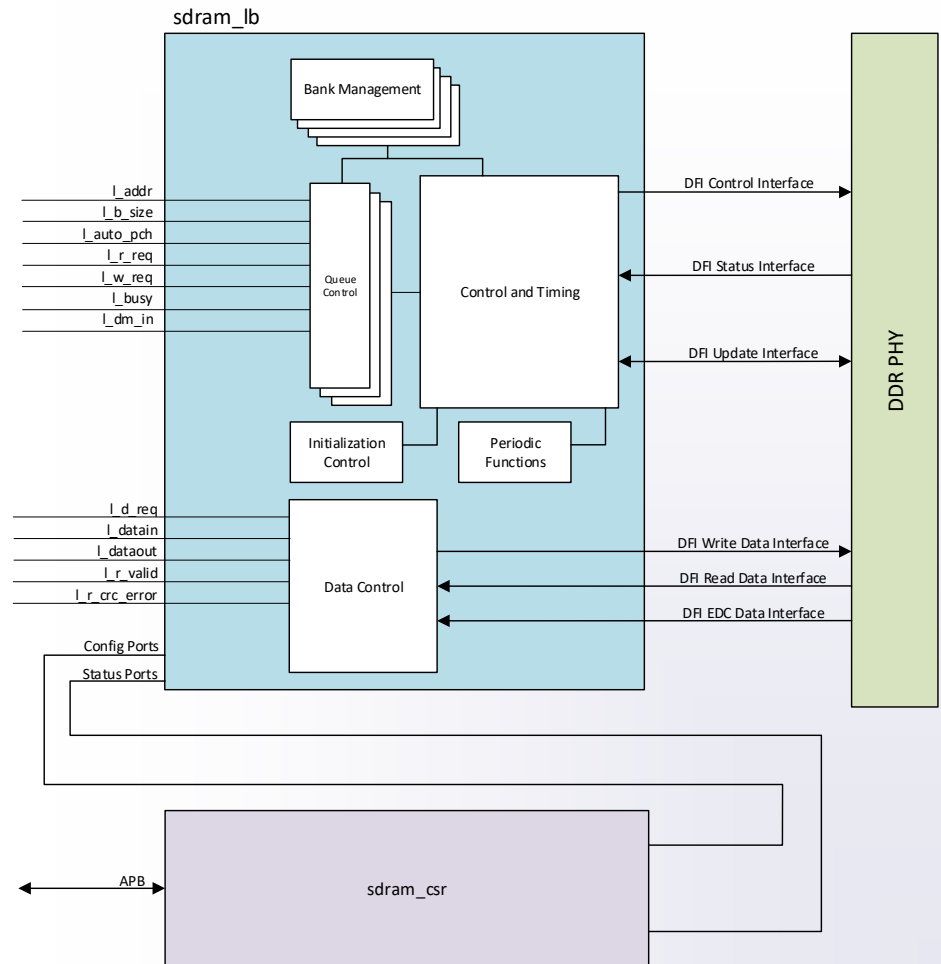


Product Highlights

- Supports GDDR6 SGRAM up to 18 Gbit/s/pin GDDR6 operation
- Can handle two x16 GDDR6 channels with one controller or independently with two controllers
- Supports GDDR6 x16 or x8 clamshell modes
- Queue based interface optimizes performance and throughput
- Maximizes memory bandwidth and minimize latency via Look-Ahead command processing
- Automatic retry on transactions where EDC error detected
- Full run-time configurable timing parameters and memory settings
- Supports automatic and controller-initiated training
- DFI Compatible (with extensions for GDDR6)
- Full set of Add-On Cores available including In-line ECC Core
- Supports AXI, OCP or Native Interface to user logic
- Delivered fully integrated and verified with target GDDR6 PHY
- Minimal ASIC gate count
- Source code available
- Customization and Integration services available

GDDR6 Controller Core Block Diagram



Product Overview

Northwest Logic's GDDR6 Controller Core is designed for use in applications requiring high memory throughput, high clock rates and full programmability.

The core accepts commands using a simple local interface and translates them to the command sequences required by GDDR6 SGRAM devices. The core also performs all initialization, refresh and power-down functions.

The core uses bank management techniques to monitor the status of each GDDR6 SGRAM bank (up to 16 banks managed concurrently). Banks are only opened or closed when necessary, minimizing access delays.

The core queues up multiple commands in the command queue. This enables optimal bandwidth utilization for both short transfers to highly random address locations as well as longer transfers to contiguous address space. The command queue is also used to opportunistically perform look-ahead activates, precharges and auto-precharges further improving overall throughput.

The core supports all GDDR6 SGRAM features, including: x16, x8 or x8 clamshell modes, error detection code (EDC), tracking of link error statistics, data bus inversion (DBI) and CA bus inversion (CABI).

Add-On Cores such as a Multi-Port Front-End, Reorder Core or In-line ECC Core can be optionally delivered with the core. The core is delivered fully integrated and verified with the target GDDR PHY. Northwest Logic supports a broad range of third party GDDR PHY. Contact Northwest Logic for more info.

Northwest Logic also provides IP Core customization services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Testbench (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates