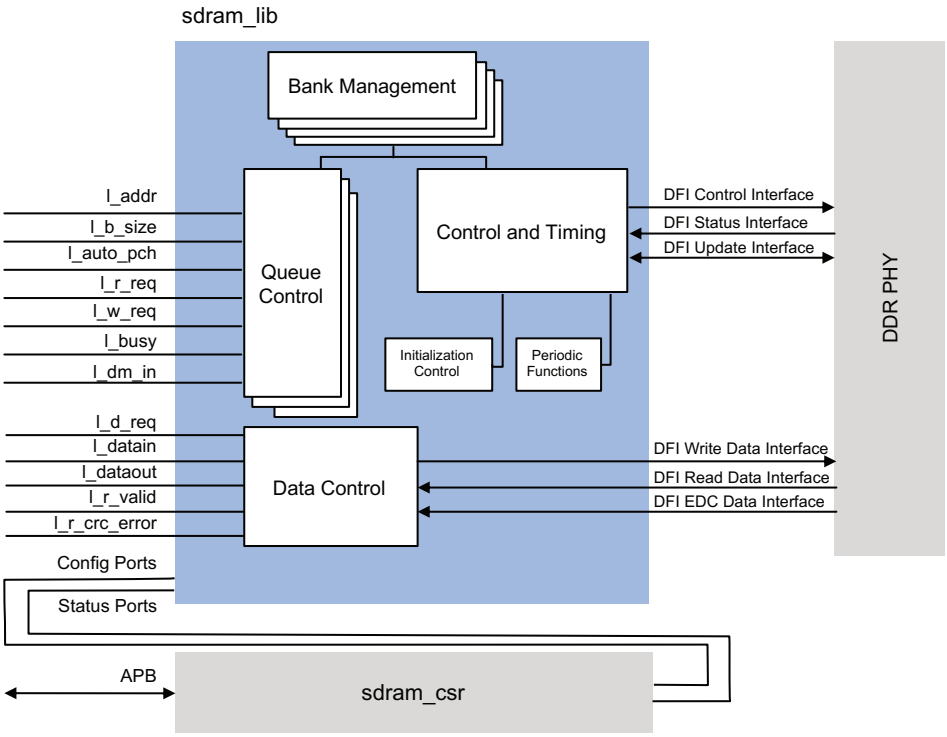
GDDR6 Controller Core

The Northwest Logic GDDR6 controller core is designed for use in applications requiring high memory throughput including graphics, advanced driver assistance systems (ADAS), high performance computing (HPC), data center, artificial intelligence (AI) and machine learning (ML).

GDDR6 Controller Core Block Diagram



Highlights

- Up to 20 Gbps per pin operation
- Can handle two x16 channels
- Queue-based interface optimizes performance
- Maximizes memory bandwidth and minimizes latency via Look-Ahead command processing
- Supports clamshell mode
- DFI compatible
- Supports AXI, OCP or native interface to user logic

Protocol Compatibility

Standards	Data Rates (Gbps)
GDDR6	12, 14, 16, 18, 20

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

Northwest Logic's GDDR6 Controller Core is designed for use in applications requiring high-memory throughput, high clock rates and full programmability.

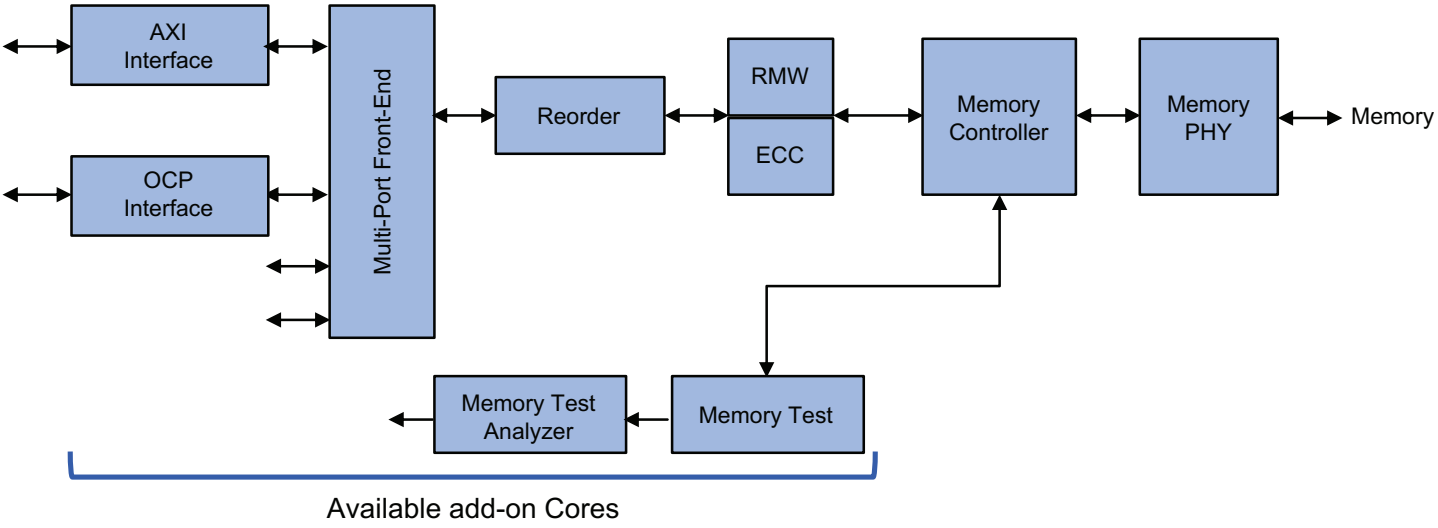
The core accepts commands using a simple local interface and translates them to the command sequences required by GDDR6 SGRAM devices. The core also performs all initialization, re-fresh and power-down functions.

The core uses bank management techniques to monitor the status of each GDDR6 SGRAM bank (up to 16 banks managed concurrently). Banks are only opened or closed when necessary, minimizing access delays.

The core queues up multiple commands in the command queue. This enables optimal bandwidth utilization for both short transfers to highly random address locations as well as longer transfers to contiguous address space. The command queue is also used to opportunistically perform look-ahead activates, precharges and auto-precharges further improving overall throughput.

The core supports all GDDR6 SGRAM features, including: x16, x8 or x8 clamshell modes, error detection code (EDC), tracking of link error statistics, data bus inversion (DBI) and CA bus inversion (CABI).

Add-On Cores



Optional Cores and Services

Add-On cores such as a Multi-Port Front-End, Reorder core or In-line ECC core are available as options. Customization and integration services are also available.

Features

- Supports up to 20 Gbps per pin operation
- Can handle two x16 GDDR6 channels with one controller or independently with two controllers
- Supports x8 or x16 clamshell mode
- Queue-based interface optimizes performance and throughput
- Maximizes memory bandwidth and minimizes latency via Look-Ahead command processing
- Automatic retry on transactions where EDC error detected
- Full run-time configurable timing parameters and memory settings
- Supports automatic and controller-initiated training
- DFI compatible (with extensions for GDDR6)
- Full set of Add-On cores available including *in-line ECC* core
- Supports AXI, OCP or native interface to user logic
- Delivered fully integrated and verified with target GDDR6 PHY
- Minimal ASIC gate count
- Source code available
- Delivered fully integrated and verified with target GDDR6 PHY
- Customization and integration services available

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