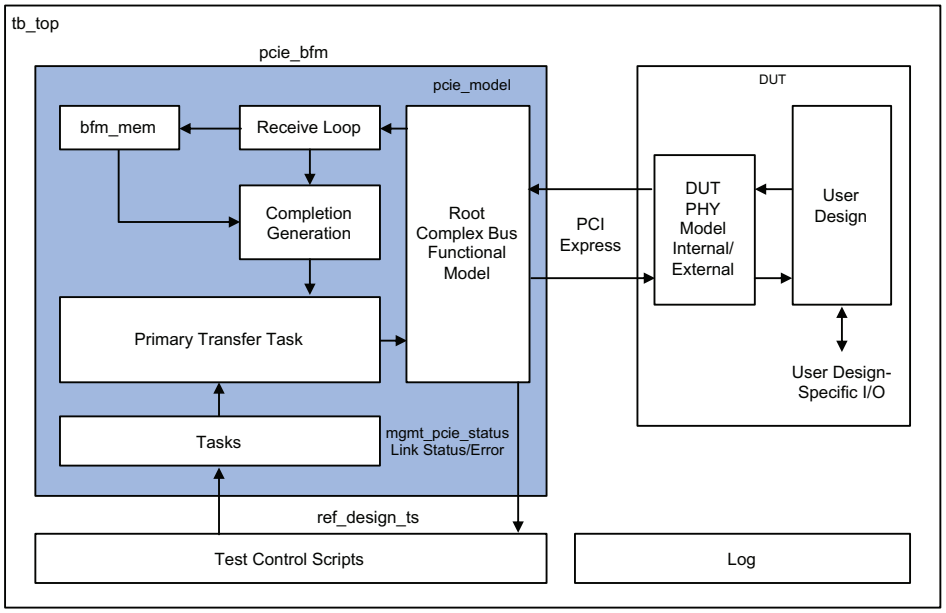
Expresso Testbench

The Northwest Logic's Expresso Testbench emulates a Root Complex device enabling simulation of a PCI Express design.

Expresso Testbench Block Diagram



Overview

The Northwest Logic Expresso Testbench emulates a Root Complex device enabling simulation of PCIe design.

Root Complex master requests are generated using simple test control scripts. A basic set of test cases is included with the suite to generate standard PCIe transactions including configuration, data tansfers, DMA and interrupts. DUT master requests receive automatic responses including completion responses.

Root Complex memory regions are modelled and used to store data sent to and received from the DUT. Data stored in these regions can be automatically checked for proper operation.

Root Complex physical and data-link layer functions are performed including error detection and correction.
Transaction-layer traffic is logged and displayed in a user-friendly format.

The fast setup and operation of the Expresso Testbench allows for quick and comprehensive simulations of designs including Northwest Logic PCI Express cores.

The Expresso Testbench is not a PCIe full-compliance suite. Rambus recommends the use of the Avery Logic PCI-Xactor PCI Express Compliance suite for ASIC validation.

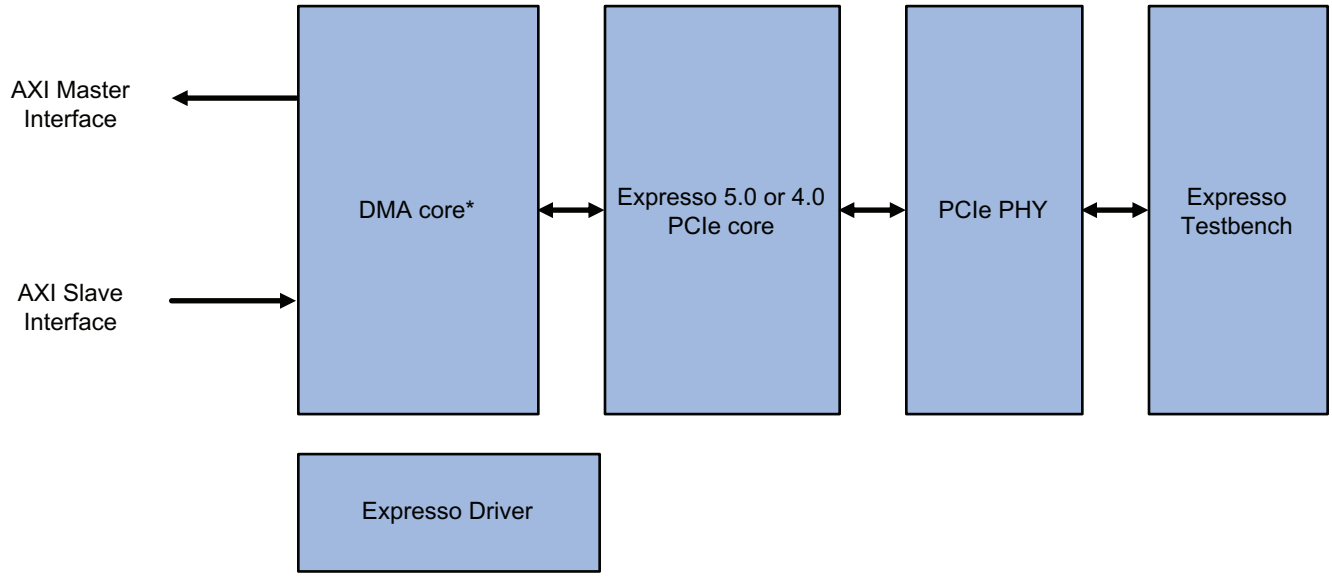
Highlights

- Emulates a Root Complex device for PCIe design simulation
- Generates Root Complex master requests via test scripts
- Automatically responds to DUT master requests
- Performs automatic data logging and checking
- Designed for quick out-of-the-box setup and use
- Provides fast simulation speed
- Complies with PCIe base specification 4.0/3.0/2.1/1.1
- Provided as source code

Deliverables

- Testbench (source code) excluding Root Complex BFM
- Documentation
- Expert technical support
- Maintenance updates

PCI Express Solution



*Options include the Expresso DMA Bridge core, DMA Back-End core or AXI DMA Back-End core

PCI Express Platform

Rambus, joined by the team at Northwest Logic, offers a complete solution for PCIe applications.

Features

- Emulates a Root Complex device for PCIe design simulation
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