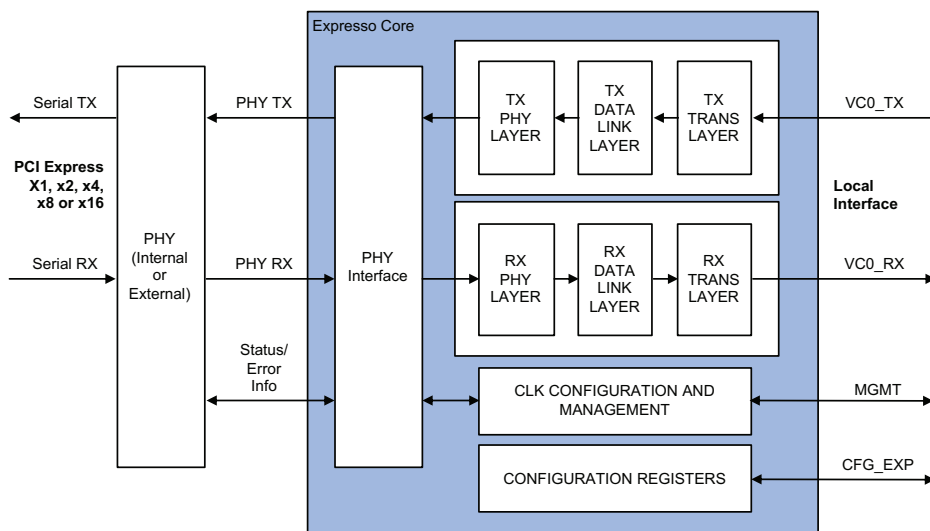


# Expresso 5.0 Core

The Northwest Logic Expresso 5.0 core is designed for maximum performance and ease of use for PCI Express® (PCIe) 5.0 applications. It is backwards compatible with PCIe 4/3/2/1 specifications.

## Expresso 5.0 Block Diagram



## Highlights

- x16, x8, x4, x2, x1 lane support
- 1-8 Physical Function support
- SR-IOV support up to 255 Virtual Functions
- Endpoint, Root Port, Upstream Switch Port, Downstream Switch Port, Bifurcation support
- 32, 64, 128, 256 and 512-bit core width support
- Full Transaction Layer (TL), Partial TL and TL Bypass interface options available
- Flexible equalization algorithms

## Protocol Compatibility

Standards	Data Rates (Gbps)
PCIe 5.0	32, 16, 8, 5, 2.5

## Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

## Overview

Northwest Logic Expresso 5.0 core is designed for maximum performance and ease of use for PCIe 5.0 applications. It is backwards compatible with PCIe 4/3/2/1 specifications.

The Expresso 5.0 Core separately, or in combination with the Northwest Logic family of DMA cores and DMA drivers, provides the maximum system throughput on a PCIe link.

The core is specifically designed for ease of use including full receive packet decoding, complete error handling, automatic handling of PCIe message packets and comprehensive system-debug and link monitoring support.

The core is delivered integrated and verified with the user's target PHY. A complete list of supported PHYs is available on

request. To accelerate simulations, the core is also delivered integrated with a fast-simulating behavioral PHY.

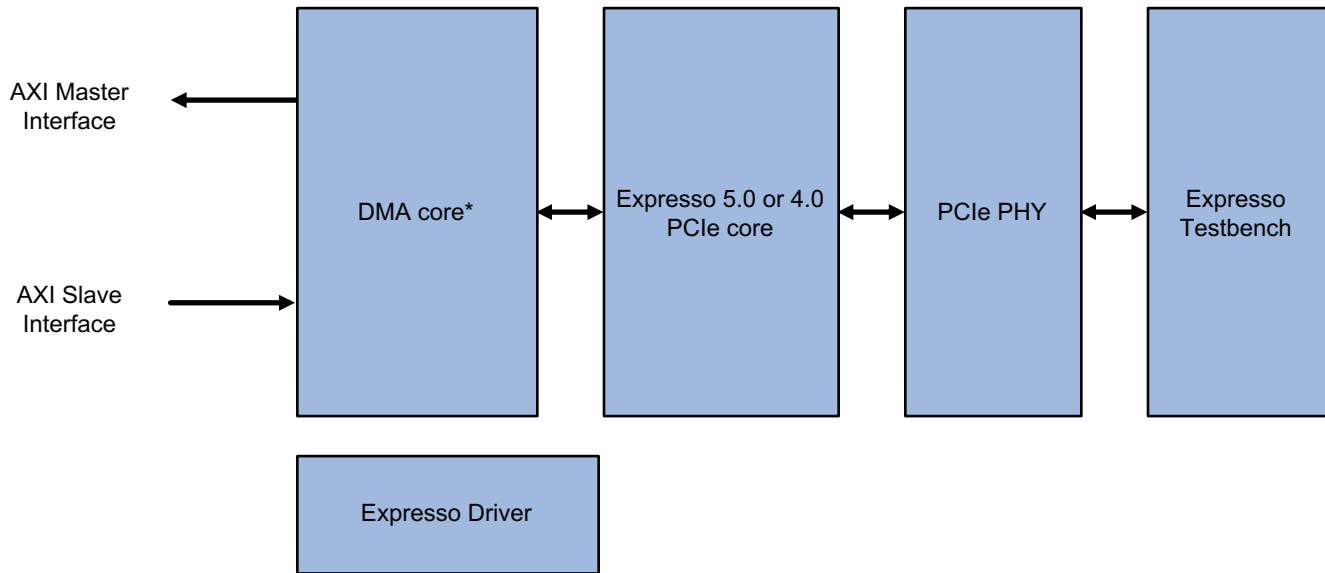
The core is provided with the Expresso Testbench which provides a PCIe Bus Functional Model.

The core is compliant with the current version of the PCIe Base Specification 5.0. The core has been extensively validated with the Avery Design Systems PCI-Xactor PCIe Compliance Suite and Northwest Logic Expresso Testbench.

IP Core customization services are also available.



## PCI Express Solution



\*Options include the Expresso DMA Bridge core, DMA Back-End core or AXI DMA Back-End core

### PCI Express Platform

Rambus, joined by the team at Northwest Logic, offers a complete solution for PCIe applications.

### Features

- High-performance, easy-to-use core
- PCIe 5.0 specification compliant; backward compatible with PCIe 4/3/2/1
- x16, x8, x4, x2, x1 lane support
- 32, 16, 8, 5 and 2.5 Gbps SERDES support
- 1-8 Physical Function support
- SR-IOV support with up to 255 Virtual Functions
- Endpoint, Root Port, Upstream Switch Port, Downstream Switch Port, Bifurcation support
- 32, 64, 128, 256, and 512-bit core width support
- Flexible equalization algorithms
- Full Transaction Layer (TL), Partial TL and TL Bypass interface options available
- Comprehensive diagnostics and debug status
- AER, ECRC, MSI-X, MSI, Lane Reversal support, L1 PM substates, SRIS, ECC/Parity Protection
- Delivered integrated and verified with target PCIe PHY
- Fully validated
- Source code available
- Customization and integration services available

[rambus.com/controllers](https://rambus.com/controllers)

