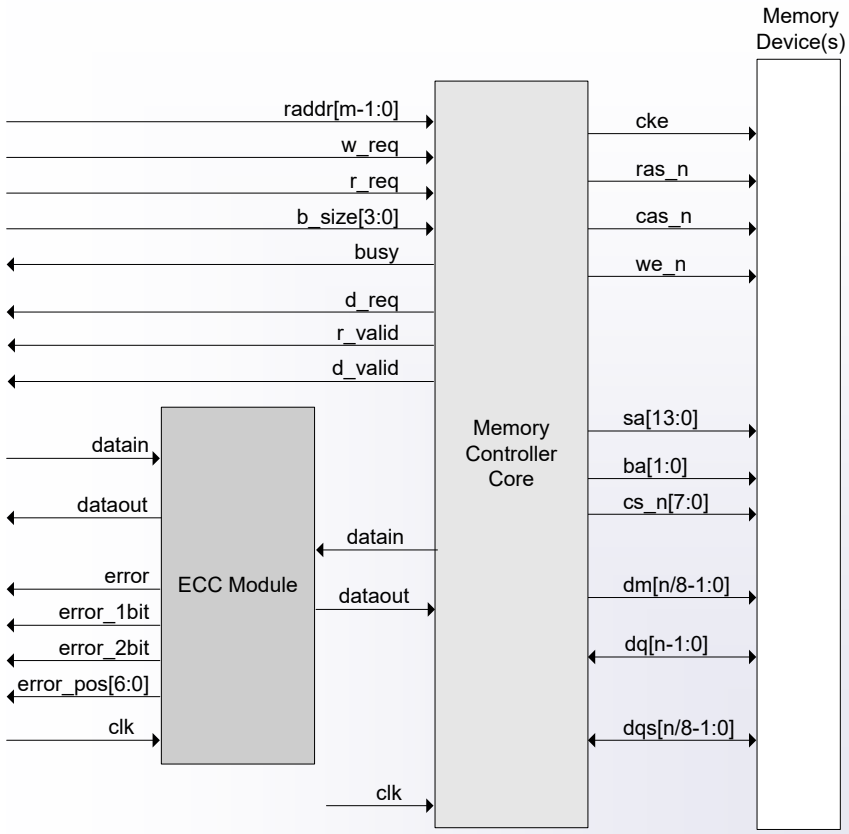
ECC Core

Product Highlights

- Implements standard DRAM Single Error Correction (SEC) and Double Error Detection (DED) algorithm
- Generates an 8 bit ECC word for a 64 bit data bus
- Error flags indicate what type of error occurred (1-bit or 2-bit)
- Bit position of the error is provided for single-bit errors
- Minimal ASIC gate count
- Broad range of ASIC and FPGA platforms supported
- Source code available
- Customization and Integration services available

Block Diagram



Product Overview

Northwest Logic's Error Correction Coding (ECC) Core implements the standard Hamming Code based DRAM Single Error Correction (SEC) and Double Error Detection (DED) algorithm. This algorithm generates an 8 bit ECC word for a 64 bit data bus.

The core consists of an ECC generation path as well as ECC detection and correction. ECC correction is possible for single bit errors occurring in one of combined 72 data and check bits. ECC detection is possible for errors in two of the combined 72 data and check bits.

Various status information is provided to the user including whether an error was detected on a single bit or two bits. The bit position of the error is provided for the case of a single bit errors.

The Read-Modify-Write (RMW) Core can be used in conjunction with the ECC Core when dealing with misaligned bursts. An ECC code word must be calculated over an entire data word. Misaligned bursts can have partial data words at the front and back end of the burst.

To calculate the correct ECC code word, the Read-Modify-Write Core forms the correct starting and ending data words by reading the existing data words and combining them appropriately with the new partial data words.

Northwest Logic also provides IP Core customization services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Testbench (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates