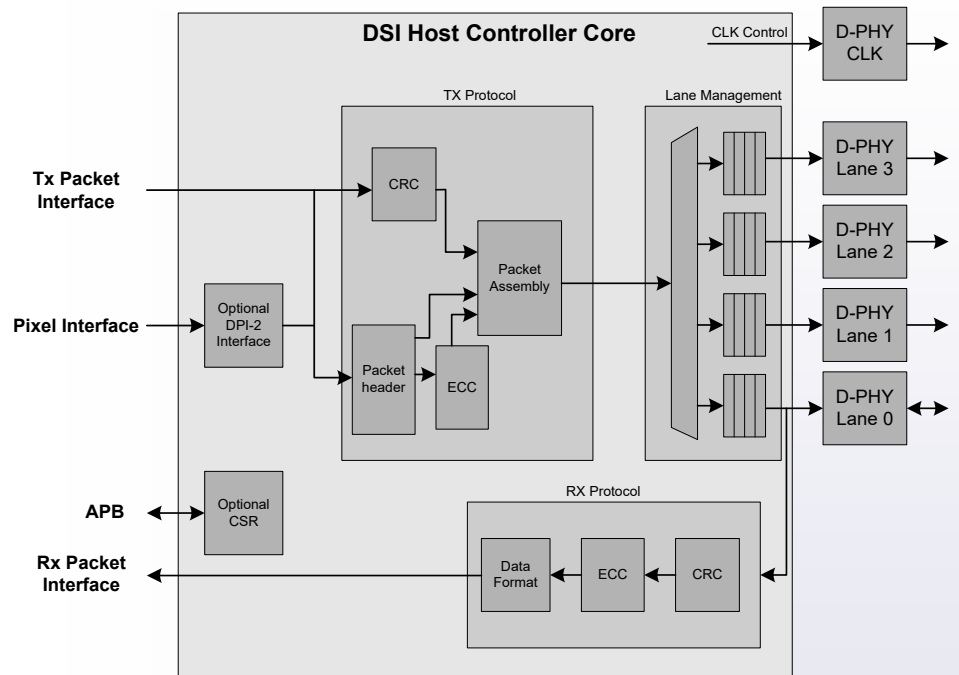


Product Highlights

- Fully DSI standard compliant
- 32 bit core width
- Host (Tx) and Peripheral (Rx) versions
- 1-4, 2.5+ Gbit/s D-PHY data lane support
- Support for all data types
- Easy to use packet interface
- Optional DPI data interface
- Delivered fully integrated and verified with target MIPI PHY
- Provided with a MIPI DSI Testbench
- Minimal ASIC gate count
- Source code available
- Customization and Integration services available
- Complete FPGA-based demonstration system available

Block Diagram (Host Version)



Product Overview

The DSI Controller Core is part of Northwest Logic's MIPI Solution. This solution is designed to achieve maximum MIPI throughput while being easy to use.

The core has a 32 bit core width. Consequently, it can support 1-4 D-PHY data lanes (8 bit PPI).

The core implements all three layers defined by the DSI standard: Pixel to Byte Packing, Low Level Protocol, and Lane Management and is fully compliant with the DSI standard. Separate Host (Tx) and Peripheral (Rx) versions of the core are provided.

The core's native interface provides an easy-to-use data and control/status packet interfaces. The data interfaces provided with optional DPI interface adapter. The core supports command and video modes and all data types.

The core is delivered fully integrated and verified with the user's target D-PHY. Contact Northwest Logic for a complete list of supported PHYs.

The core is also provided with the DSI Testbench which provides a DSI Bus Functional Model.

Northwest Logic also offers a DSI Demonstration System which includes an FPGA Board, MIPI Interface Card and MIPI Display. Contact Northwest Logic for more information.

Northwest Logic also provides a complete set of quick-turn design services including IP Customization and Logic, Board, Software Development services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Testbench (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates