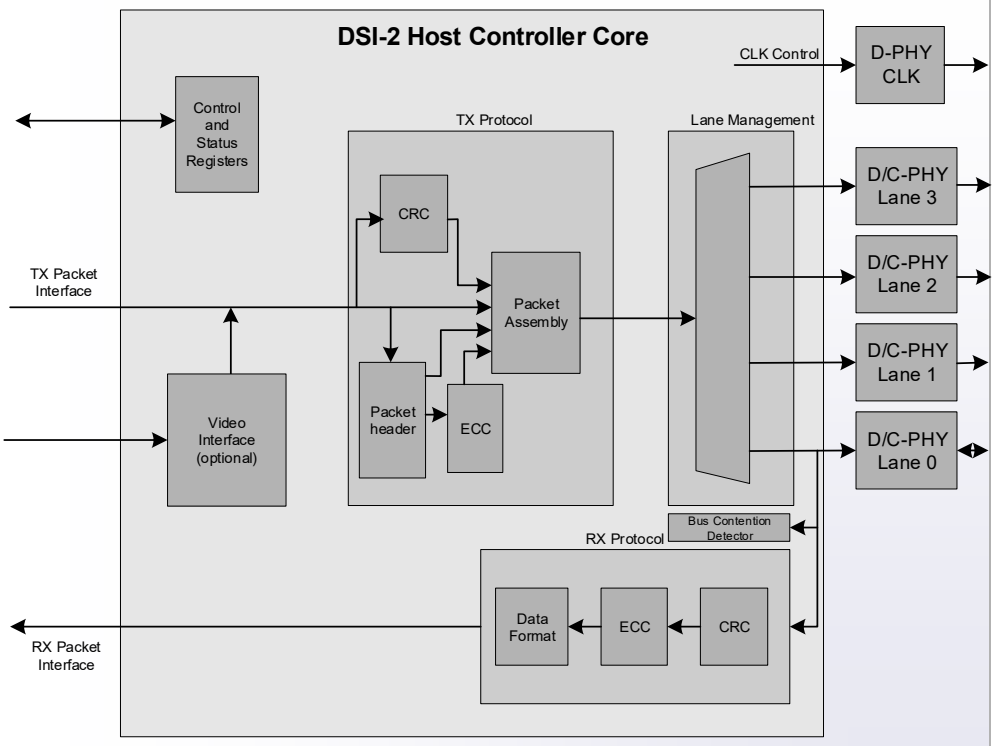
DSI-2 Controller Core

Product Highlights

- Fully DSI-2/DSI standard compliant
- 64 and 32 bit core widths
- Host (Tx) and Peripheral (Rx) versions
- 1-4, 2.5+ Gbit/s D-PHY data lane support
- 1-4, 2.5+ Gsym/s C-PHY lane (trio) support
- Support for all data types
- Easy to use native interface
- Optional DSI-2 video interface
- Delivered fully integrated and verified with target MIPI PHY
- Provided with a DSI-2 Testbench
- Minimal ASIC gate count
- Source code available
- Customization and Integration services available
- Complete FPGA-based demonstration system available

Block Diagram (Host Version)



Product Overview

The DSI-2 Controller Core is Northwest Logic's second generation DSI controller core. It is further optimized for high performance, low power and small size.

It is available in 64 and 32 bit core widths. The 64 bit core width can support 1-4 D-PHY data lanes (8 bit PPI) and 1-4 C-PHY lanes (16 bit PPI). The 32 bit core width an support 1-4 D-PHY data lanes (8 bit PPI) and 1-2 C-PHY lanes (16 bit PPI)

The core implements all three layers defined by the DSI-2 standard: Pixel to Byte Packing, Low Level Protocol, and Lane Management and is fully compliant with the DSI-2 standard. Separate Host (Tx) and Peripheral (Rx) versions of the core are provided.

The core's native interface provides an easy-to-use data and control/status packet interfaces. The data interfaces provided with optional DSI-2 Video Interface . The interface supports command and video modes and all data types.

The core is delivered fully integrated and verified with the user's target D/C-PHY. Contact Northwest Logic for a complete list of supported PHYs.

The core is also provided with the DSI-2 Testbench which provides a DSI-2 Bus Functional Model.

Northwest Northwest Logic also provides IP Core customization services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Testbench (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates