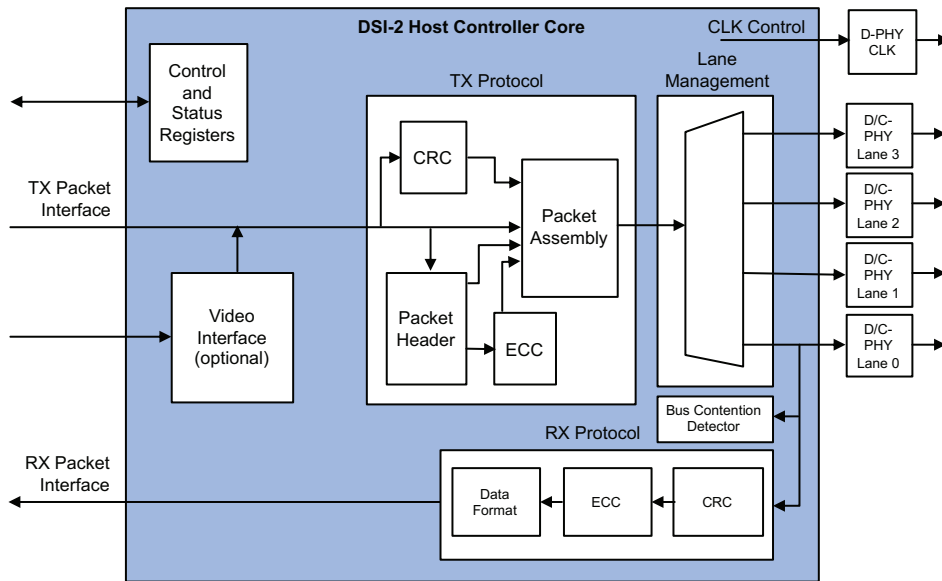


DSI-2 Controller Core

The Northwest Logic DSI-2 controller core is a second-generation DSI core optimized for high performance, low power and small size.

DSI-2 Controller Block Diagram (Host Version)



Highlights

- Fully DSI-2/DSI standard compliant
- 64 and 32-bit core widths
- Host (Tx) and Peripheral (Rx) versions
- 1-4, 2.5+ Gbps D-PHY data lanes
- 1-4, 2.5+ Gsym/s C-PHY lane (trio)
- Supports all data types
- Easy-to-use native interface
- Delivered fully integrated and verified with target MIPI PHY
- Provided with DSI-2 testbench

Protocol Compatibility

Standards	Data Rate
DSI-2/DSI	2.5+ Gbps/lane

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic DSI-2 Controller Core is optimized for high-performance, low power and small size.

It is available in 64 and 32-bit core widths. The 64-bit core width supports 1-4 D-PHY data lanes (8-bit PPI) and 1-4 C-PHY lanes (16-bit PPI). The 32-bit core width supports 1-4 D-PHY data lanes (8-bit PPI) and 1-2 C-PHY lanes (16-bit PPI).

The core is fully compliant with the DSI-2 standard and implements all three layers defined therein: Pixel to Byte Packing, Low Level Protocol, and Lane Management. Separate Host (Tx) and Peripheral (Rx) versions of the core are available.

The core's native interface provides easy-to-use data and control/status packet interfaces. The data interface includes an optional DSI-2 video interface. The interface supports command and video modes and all data types.

The core is delivered fully integrated and verified with the user's target D/C-PHY. Please contact Rambus for a complete list of supported PHYs.

The core is also provided with the DSI-2 Testbench which provides a DSI-2 Bus Functional Model.

Features

- Fully DSI-2/DSI standard compliant
- 64 and 32-bit core widths
- Host (Tx) and Peripheral (Rx) versions
- Supports 1-4, 2.5+ Gbps D-PHY data lanes
- Supports 1-4, 2.5+ Gsym/s C-PHY lane (trio)
- Supports all data types
- Accepts MIPI compliant DPI-2 set of signals
- Easy-to-use native interface
- Delivered fully integrated and verified with target MIPI PHY
- Provided with DSI-2 testbench
- Minimal ASIC gate count
- Source code available
- Customization and integration services available
- Complete FPGA-based demonstration system available

rambus.com/controllers

