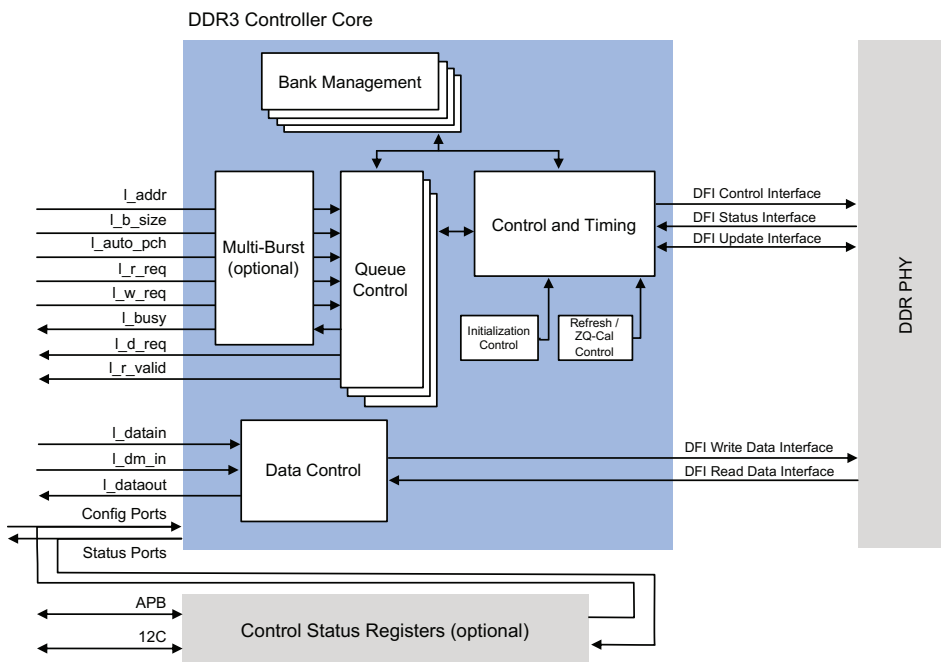


DDR3 Controller Core

The Northwest Logic DDR3 controller core is designed for high memory throughput, high clock rates, and full programmability in computing and networking applications.

DDR3 Controller Core Block Diagram



Highlights

- Maximizes bus efficiency via look-ahead command processing, bank management, auto-precharge and additive latency support
- Supports full-rate and half-rate clock operation
- Supports ODT, dynamic ODT, 2T timing and write leveling calibration
- DFI compatible
- Multi-mode controller support

Protocol Compatibility

Standards	Data Rates (Mbps)
DDR3	800 to 2133

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

Northwest Logic's DDR3 Controller Core is designed for use in applications requiring high memory throughput, high clock rates and full programmability.

The core accepts commands using a simple local interface and translates them to the command sequences required by DDR3 SDRAM devices. The core also performs all initialization, refresh and power-down functions.

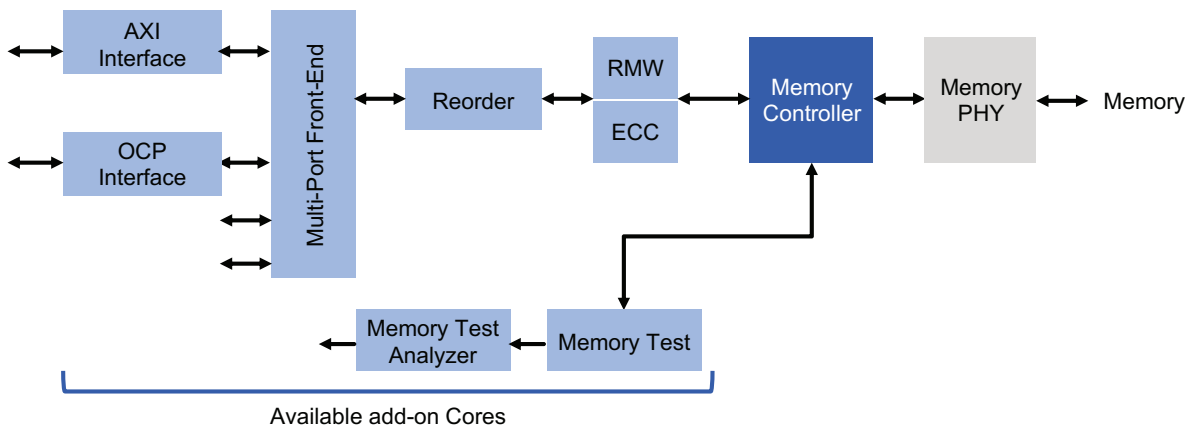
Bank management modules monitor the status of each SDRAM bank. Banks are only opened or closed when necessary, minimizing access delays. Up to 32 banks can be managed at one time.

Multiple commands are queued enabling optimal bandwidth utilization for both short transfers to highly random address locations as well as longer transfers to contiguous address space. The command queue is also used to opportunistically perform look-ahead activates, precharges and auto-precharges further improving overall throughput.

The core is provided with run-time programmable inputs for all memory timing parameters and configuration settings. This ensures compatibility with all DDR3 SDRAM configurations. ODT, dynamic ODT, 2T timing and write leveling calibration are supported.



Add-On Cores



Optional Cores and Services

Add-On cores such as a Multi-Port Front-End, Reorder core, and out-of-band ECC cores are available as options. Customization and integration services are also available.

Features

- Maximizes bus efficiency via look-ahead command processing, bank management, auto-precharge and additive latency support
- Latency minimized via parameterized pipelining
- Achieves high clock rates with minimal routing constraints
- Supports full-rate and half-rate clock operation
- Multi-mode controller support
- Full run-time configurable timing parameters and memory settings
- Supports ODT, dynamic ODT, 2T timing and write leveling calibration
- DFI compatible
- Full set of Add-On cores available
- Minimal ASIC gate count
- Broad range of ASIC and FPGA platforms supported
- Delivered fully integrated and verified with target PHY
- Source code available
- Customization and integration services available

rambus.com/controllers

