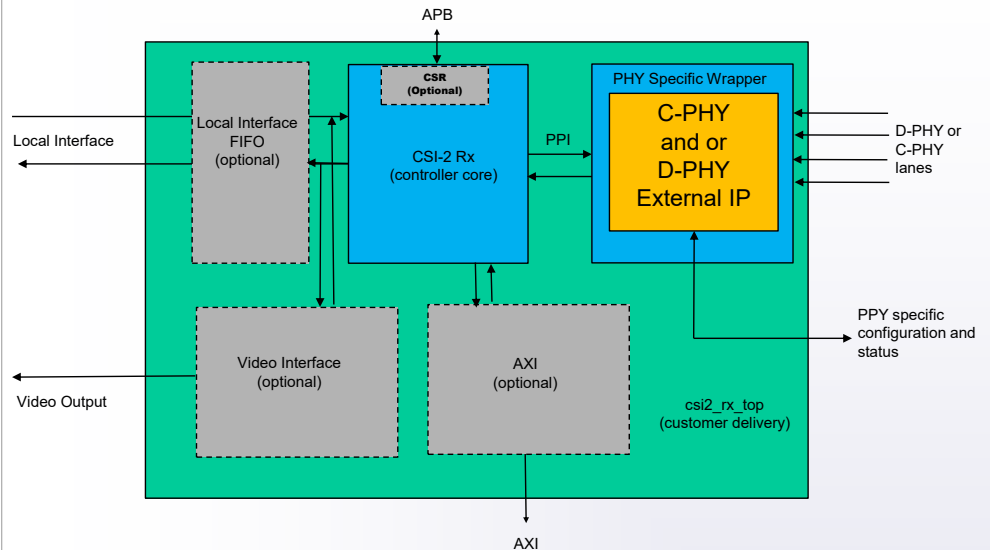


Product Highlights

- Fully CSI-2 standard compliant
- 64 and 32 bit core widths
- Transmit and Receive versions
- 1-8, 2.5+ Gbit/s D-PHY data lane support
- 1-4, 2.5+ Gsym/s C-PHY lane (trio) support
- Support for all data types
- Easy to use pixel-based user interface
- Optional AXI interface
- Optional Video Interface
- Delivered fully integrated and verified with target MIPI PHY
- Provided with a CSI-2 Testbench
- Minimal ASIC gate count
- Source code available
- Customization and Integration services available
- Complete FPGA-based demonstration system available

Block Diagram (Receive Version)



Product Overview

The CSI-2 Controller Core V2 is Northwest Logic's second generation CSI-2 controller core. It is further optimized for high performance, low power and small size.

It is available in 64 and 32 bit core widths. The 64 bit core width can support 1-8 D-PHY data lanes (8 bit PPI) and 1-4 C-PHY lanes (16 bit PPI). The 32 bit core width can support 1-4 D-PHY data lanes (8 bit PPI) and 1-2 C-PHY lanes (16 bit PPI)

The core implements all three layers defined by the CSI-2 standard: Pixel to Byte Packing, Low Level Protocol, and Lane Management and is fully compliant with the CSI-2 standard. Separate Transmit (Tx) and Receive (Rx) versions of the core are available.

The core's Local Interface is an easy to use pixel based interface (single, double, quad, octal pixel wide). An optional AXI interface is available for the CSI-2 Rx Controller Core. An optional Hsync/Vsync Video Interface is also available.

The core is delivered fully integrated and verified with the user's target D/C-PHY. Contact Northwest Logic for a complete list of supported PHYs.

The core is also provided with the CSI-2 Testbench which provides a CSI-2 Bus Functional Model.

Northwest Logic also provides IP Core customization services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Testbench (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates