CSI-2 Controller Core V2

The Northwest Logic CSI-2 controller core is a second-generation CSI-2 core optimized for high performance, low power and small size.

Overview

The Northwest Logic CSI-2 Controller Core V2 is optimized for high-performance, low power and small size.

It is available in 64 and 32-bit core widths. The 64-bit core width supports 1-8 D-PHY data lanes (8-bit PPI) and 1-4 C-PHY lanes (16-bit PPI). The 32-bit core width supports 1-4 D-PHY data lanes (8-bit PPI) and 1-2 C-PHY lanes (16-bit PPI).

The core is fully compliant with the CSI-2 standard and implements all three layers defined therein: Pixel to Byte Packing, Low Level Protocol, and Lane Management. Separate Transmit (Tx) and Receive (Rx) versions of the core are available.

The core’s local interface provides an easy-to-use pixel based interface (single, double, quad, octal pixel wide). An optional AXI interface is available for the CSI-2 Rx Controller Core. An optional Hsync/Vsync video interface is also available.

The core is delivered fully integrated and verified with the user’s target D/C-PHY. Please contact Rambus for a complete list of supported PHYs.

The core is also provided with the CSI-2 Testbench which provides a CSI-2 Bus Functional Model.

Highlights

• Fully CSI-2 standard compliant
• 64 and 32-bit core widths
• Transmit and Receive versions
• 1-8, 2.5+ Gbps D-PHY data lanes
• 1-4, 2.5+ Gsym/s C-PHY lane (trio)
• Optional video interface
• Easy-to-use pixel-based interface
• Delivered fully integrated and verified with target MIPI PHY
• Provided with CSI-2 testbench

Protocol Compatibility

<table>
<thead>
<tr>
<th>Standards</th>
<th>Data Rate</th>
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<tbody>
<tr>
<td>CSI-2</td>
<td>2.5+ Gbps/lane</td>
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Deliverables

• Core (source code)
• Testbench (source code)
• Complete documentation
• Expert technical support
• Maintenance updates
Features

- Fully CSI-2 standard compliant
- 64 and 32-bit core widths
- Transmit and Receive versions
- Supports 1-8, 2.5+ Gbps D-PHY data lanes
- Supports 1-4, 2.5+ Gsym/s C-PHY lane (trio)
- Supports all data types
- Easy-to-use pixel-based interface
- Optional AXI interface (Rx only)

- Optional video interface
- Delivered fully integrated and verified with target MIPI PHY
- Provided with CSI-2 testbench
- Minimal ASIC gate count
- Source code available
- Customization and integration services available
- Complete FPGA-based demonstration system available