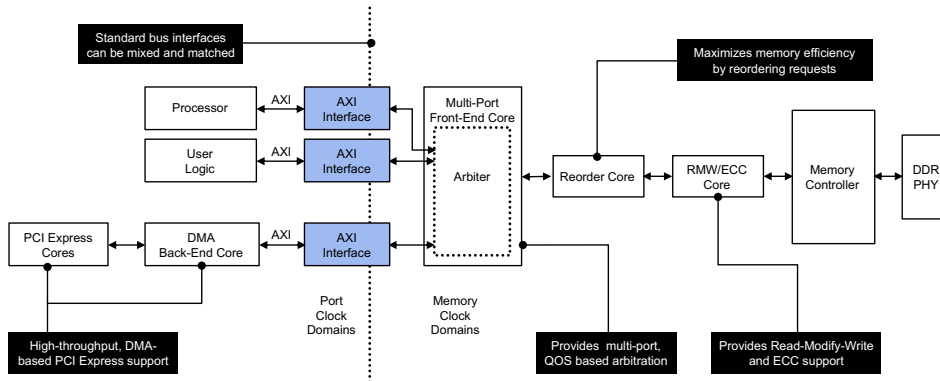


AXI Interface Core

The Northwest Logic AXI Interface core is designed for use in applications requiring ARM's Advanced eXtensible Interface (AXI).

AXI Interface Core Application Example



Highlights

- Provides high-performance interface to AXI
- Handles conversion of bus width/speed to memory width/speed
- Provided with a bus functional model (testbench)
- Achieves high clock rates with minimal routing constraints
- Source code available
- Customization and integration services available

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

Northwest Logic's AXI Interface core is designed for use in applications requiring ARM's Advanced eXtensible Interface (AXI).

The core accepts write and read requests from a Bus Master. After receiving a write request the core immediately accepts the associated write data enabling the Bus Master to proceed to the next request. The core then arranges for the data to be written into the memory. After receiving a read request, the core arranges for the data to be read from the memory and then provides it to the Bus Master.

The core handles the conversion of the bus width/speed to the memory width/speed. This enables the bus width and speed to be completely independent of the memory width and speed. The core can be used in a single port configuration connected directly to the Memory Controller core. Multiple instances of the core can be used with Northwest Logic's Multi-Port FrontEnd core. This enables a multi-port design with a mix of different types of bus interfaces to be quickly and easily created.

Northwest Logic also provides the AXI Interface core with a testbench which serves as a bus functional model.

The AXI Interface core requires the Read-Modify-Write core which is licensed separately.

Northwest Logic also provides IP Core customization services.

rambus.com/controllers

