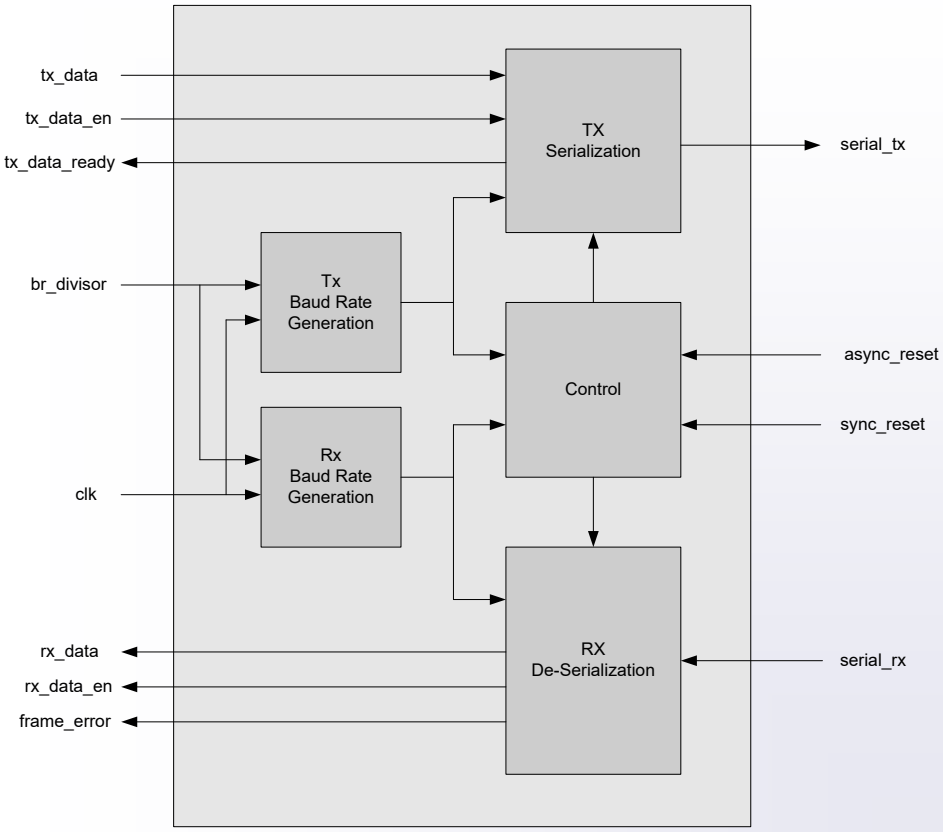
UART Lite Core

Product Highlights

- Very small size
- Specifically design for ease of use
- Simple user interface
- Programmable Tx and Rx baud rate
- 7 and 8 bit data bit support
- None, Even, Odd, Mark, Space parity bit support
- 1 or 2 stop bit support
- Frame and parity error detection
- Optional SAE J1708 support available
- Can directly connect to Tx and Rx FIFOs
- Minimal ASIC gate count
- Broad range of ASIC and FPGA platforms supported
- Source code available
- Customization and Integration services available

Block Diagram



Product Overview

Northwest Logic's UART Lite Core eliminates the extra logic and complexity of a standard 16C550 UART to provide a core which is very small, easy to use and customizable if needed. The core's small size makes it particularly useful in multiple serial port designs.

The core supports all of the standard UART features including programmable Tx and Rx baud rates, 7/8 bit data, N/E/O/M/S parity bit and 1/2 stop bits. The core also provide frame and parity error detection. The core also optionally supports SAE J1708.

The Tx and Rx FIFOs are not integrated into the core. Instead the core can be directly connected to external FIFOs. This enables the designer to use FIFOs that are set to the optimal depth. Often times, FIFO which are deeper or shallower than the standard 16-word 16C550 FIFOs are desirable. This also eliminates wasting logic blocks to implement the FIFOs.

Northwest Logic also provides IP Core customization services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Testbench (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates