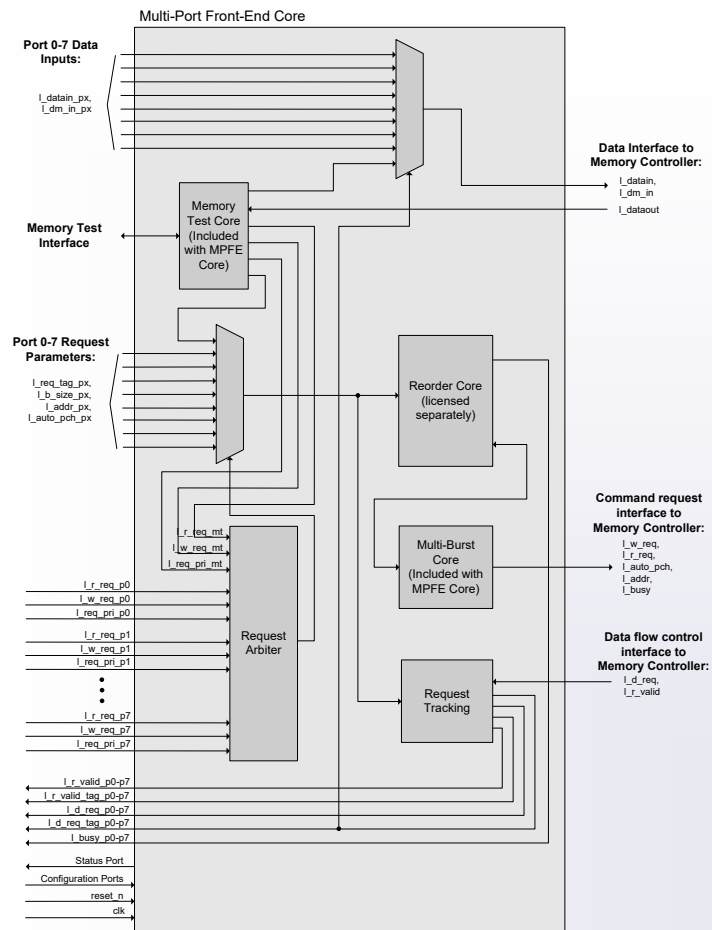


Product Highlights

- Provides a multi-port interface to Northwest Logic's Memory Controller Cores
- Supports up to 32 user ports
- Performs priority and Quality Of Service (QoS) based arbitration
- Prevents request stalling using request timeout
- Automatically translates long burst requests into multiple requests matching the memory's native burst length
- Memory Test and Reorder Core can be optionally added
- Achieves high clock rates with minimal routing constraints
- Minimal ASIC gate count
- Broad range of ASIC and FPGA platforms supported
- Source code available
- Customization and Integration services available

Block Diagram



Product Overview

The Multi-Port Front-End Core provides a multi-port interface to Northwest Logic's Memory Controller Cores.

Each user request is provided with its own request priority. The arbiter selects requests based on priority and then round robin arbitration. The arbiter can also perform Quality Of Service (QoS) based arbitration. In this mode, the arbitration results in each port receiving a specified amount of memory bandwidth. Each port also has a programmable time out period. Once a request times out, its priority is raised to the highest level ensuring its quick execution.

The Multi-Port Front-End Core includes the Multi-Burst Core. It automatically translates long burst requests into multiple requests matching the memory's native burst length. This enables read or write requests of 256 data cycles or more. The Multi-Port Front-End Core can be used with or without the Multi-Burst Core. Northwest Logic will remove the Multi-Burst Core from a delivery upon request.

The Multi-Port Front-End Core can optionally include the Memory Test Core which performs address and data testing.

The Multi-Port Front-End Core can be used with the Reorder Core to perform request reordering. The Reorder core rearranges the order of the requests coming from the Multi-Port Front-End to prioritize high priority requests and optimize memory throughput. This includes moving same bank/same row requests next to each other, same bank/ different row

requests away from each other, moving reads next to reads and write next to writes. Data coherency is maintained during the reordering operation.

Northwest Logic also provides IP Core customization services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Testbench (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates