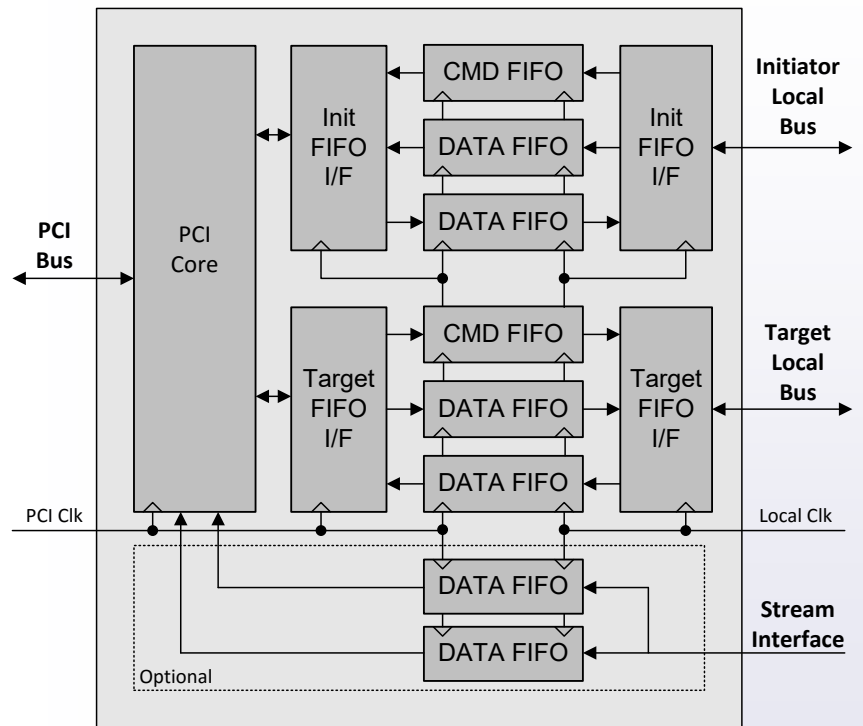


Product Highlights

- PCI Local Bus Specification Revision 3.0 compliant
- Pre-integrated with command and data FIFOs. Requires minimal PCI expertise and design effort to use.
- Provides maximum PCI throughput by supporting multiple posted writes, delayed reads, and read pre-fetching
- Fully complies with PCI Transaction and Ordering rules
- Independent FIFOs enable simultaneous PCI and Local Bus data transfers
- Optional Read Streaming Mode supports applications requiring high read data throughput
- User expandable configuration space can be loaded from EEPROM
- 33/66 MHz or 32/64 bit, Host or Peripheral, Master/Target or Target-Only versions
- Provided with a PCI-X/PCI Testbench
- Minimal ASIC gate count
- Source code available
- Customization and Integration services available

Block Diagram



Product Overview

Northwest Logic's Integrated PCI Core is specifically designed to enable a user to implement a high-performance PCI system with no additional PCI logic design. The Integrated PCI Core accomplishes this by integrating Northwest Logic's PCI Core with a high-performance back-end.

The core enables the maximum possible PCI throughput to be achieved through the use of independent FIFOs (Master Write, Target Write, Master Read, Target Read). The FIFOs support multiple posted writes, delayed reads, and read pre-fetching operations. In addition, the FIFOs enable PCI Bus and Local Bus data transfers to occur simultaneously.

The core fully complies with all PCI transaction and ordering rules in accordance with the PCI specification.

The core is available in several flavors including 32 vs. 32/64 bit, Target-Only vs. Master/Target, and Peripheral vs. Host and versions.

The core is also provided with the PCI-X/PCI Testbench which provides a PCI-X/PCI Bus Functional Model.

Northwest Logic also provides IP Core customization services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Testbench (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates